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SERIES O: SPECIFICATIONS OF MEASURING EQUIPMENT

Equipment for the measurement of digital and analogue/digital parameters

Timing jitter and wander measuring equipment for digital systems which are based on the plesiochronous digital hierarchy (PDH)

ITU-T Recommendation O.171

(Previously CCITT Recommendation)

ITU-T O-SERIES RECOMMENDATIONS

SPECIFICATIONS OF MEASURING EQUIPMENT

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ITU-T RECOMMENDATION O.171

TIMING JITTER AND WANDER MEASURING EQUIPMENT FOR DIGITAL SYSTEMS WHICH ARE BASED ON THE PLESIOCHRONOUS DIGITAL HIERARCHY (PDH)

Summary

The requirements for the characteristics of the jitter and wander measuring equipment which are described below must be adhered to in order to ensure compatibility between equipment produced by different manufacturers.

While requirements are given for the equipment, the realization of the equipment configuration is not covered and should be given careful consideration by the designer and user. In particular, it is not required that all features listed below shall be provided in one piece of equipment. Users may select those functions which correspond best to their applications.

Source

ITU-T Recommendation O.171 was revised by ITU-T Study Group 4 (1997-2000) and was approved under the WTSC Resolution No. 1 procedure on the 19th of April 1997.

Keywords

Jitter generation, jitter measurements, jitter transfer function, output jitter, tolerable input jitter, wander generation, wander measurements.

FOREWORD

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NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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Recommendation O.171

TIMING JITTER AND WANDER MEASURING EQUIPMENT FOR DIGITAL SYSTEMS WHICH ARE BASED ON THE PLESIOCHRONOUS DIGITAL HIERARCHY (PDH)

(Geneva, 1980; amended Malaga-Torremolinos, 1984; Melbourne, 1988; revised in 1997)

1 Scope

The instrumentation specified in this Recommendation will be used to measure timing jitter and wander on digital systems based on the Plesiochronous Digital Hierarchy (PDH). The instrumentation consists of a jitter measuring circuit and a test signal source. Measurements can be performed at the physical layer of PDH systems. An error-ratio meter may also be required for certain types of measurements.

Instrumentation for the measurement of jitter and wander on digital systems based on the Synchronous Digital Hierarchy (SDH) is specified in a separate O-Series Recommendation.

It is recommended that Recommendations G.823 [7] and G.824 [8] be read in conjunction with this Recommendation.

2 References

2.1 Normative references

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. All Recommendations are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations listed below. A list of the currently valid ITU-T Recommendations is regularly published.

[1] ITU-T Recommendation G.701 (1993), *Vocabulary of digital transmission and multiplexing, and Pulse Code Modulation (PCM) terms.*

[2] CCITT Recommendation G.703 (1991), *Physical/electrical characteristics of hierarchical digital interfaces*.

[3] ITU-T Recommendation G.772 (1993), *Protected monitoring points provided on digital transmission systems*.

[4] ITU-T Recommendation G.810 (1996), *Definitions and terminology for synchronization networks*.

[5] CCITT Recommendation G.811 (1988), *Timing requirements at the outputs of primary reference clocks suitable for plesiochronous operation of international digital links.*

[6] CCITT Recommendation G.812 (1988), *Timing requirements at the outputs of slave clocks suitable for plesiochronous operation of international digital links*.

[7] ITU-T Recommendation G.823 (1993), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

[8] ITU-T Recommendation G.824 (1993), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy*.

[9] CCITT Recommendation O.3 (1992), *Climatic conditions and relevant tests for measuring equipment.*

[10] ITU-T Recommendation O.150 (1996), *General requirements for instrumentation for performance measurements on digital transmission equipment.*

2.2 Bibliographical references

[11] ANSI Standard T1.102-1993, *Digital hierarchy – Electrical interfaces.*

[12] HUCKETT (P.): Performance Evaluation in an ISDN – Digital Transmission Impairments, *Radio and Electronic Engineer*, Vol. 54, No. 2, February 1984.

[13] TRISCHITTA (P.R.): Jitter Accumulation in Fibre Optic Systems, *Rutgers*, The State University of New Jersey, May 1986.

[14] TRISCHITTA (P.R.), SANUTTI (P.): The Jitter Tolerance of Fibre Optic Regenerators, *IEEE Transactions on Communications*, Vol. 35, No. 12, December 1987.

3 Definitions

This Recommendation defines the following terms (see Recommendation G.810 [4]):

3.1 (timing) jitter: The short-term variations of the significant instances of a digital signal from their ideal positions in time (where short-term implies these variations are of frequency greater than or equal to 10 Hz).

3.2 wander: The long-term variations of the significant instances of a digital signal from their ideal position in time (where long-term implies that these variations are of frequency less than 10 Hz).

4 Abbreviations

This Recommendation uses the following abbreviations.

AMI Alternate Mark Inversion

MTIE Maximum Time Interval Error

NRZ Non Return to Zero

PDH Plesiochronous Digital Hierarchy

SDH Synchronous Digital Hierarchy

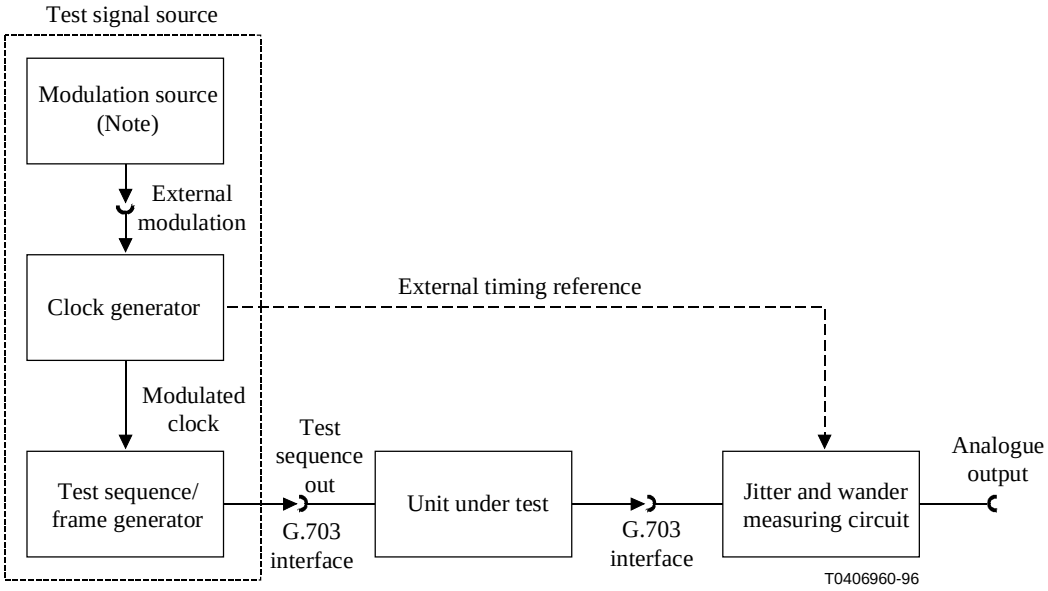
TDEV Time Deviation

TIE Time Interval Error

UI Unit Interval

5 Block diagram

Figure 1 shows the block diagram of the instrumentation in general form. The figure does not describe a specific implementation.



NOTE – The modulation source, to test to relevant G-Series Recommendations, may be provided within the clock generator and/or test sequence generator, or it may be provided separately.

Figure 1/O.171 – Simplified block diagram for measuring timing jitter and wander

6 Interfaces

6.1 Electrical interfaces

The instrumentation shall be capable of operating at one or more of the following bit rates and corresponding interface characteristics as described in the appropriate clauses of Recommendation G.703 [2]. However, for all bit rates the signal applied to the input of the jitter measuring circuit should be a nominal rectangular pulse. Other signal shapes may produce inter-symbol interference – which cannot be corrected by simple line equalization – thus affecting measurement accuracy.

a)	64	kbit/s;[1]	f)	32 064	kbit/s;
b)	1 544	kbit/s;	g)	44 736	kbit/s;
c)	6 312	kbit/s;	h)	34 368	kbit/s;
d)	2 048	kbit/s;	i)	139 264	kbit/s.
e)	8 448	kbit/s;			

As an option, the jitter measuring circuit shall be capable of measuring jitter at a clock output port when such an access is provided on digital equipment.

[1] References to 64 kbit/s relate to the co-directional interface.

6.2 Interface impedances

The jitter measuring circuit and signal source shall have a return loss as specified in Table 1[2] under the conditions listed in the Table.

Table 1/O.171 – Return loss test conditions

Bit rate (kbit/s)	Return loss (dB)	Test conditions	
64	≥ 12 ≥ 18 ≥ 14	120 Ω, non-reactive	3 kHz to 6.4 kHz 6.4 to 128 kHz 128 to 192 kHz
1 544	≥ 20	100 Ω, non-reactive	20 kHz to 1.6 MHz
2 048	≥ 12 ≥ 18 ≥ 14	75/120/130 Ω, non-reactive	51 to 102 kHz 102 to 2 048 kHz 2 048 to 3 072 kHz
6 312	≥ 20	75/110 Ω, non-reactive	100 kHz to 6.5 MHz
8 448	≥ 12 ≥ 18 ≥ 14	75 Ω, non-reactive	211 to 422 kHz 422 to 8 448 kHz 8 448 to 12 672 kHz
32 064	≥ 20	75 Ω, non-reactive	500 kHz to 40 MHz
34 368	≥ 12 ≥ 18 ≥ 14	75 Ω, non-reactive	860 to 172 040 kHz 1 720 to 34 368 kHz 34 368 to 51 550 kHz
44 736	≥ 20	75 Ω, non-reactive	500 kHz to 50 MHz
139 264	≥ 15	75 Ω, non-reactive	7 MHz to 210 MHz

7 Test signal source

Tests of digital equipment may be made with either a jittered or a non-jittered digital signal. This will require the test sequence generator, frame generator, clock generator and modulation source shown in Figure 1.

7.1 Modulation source

The modulation source, required to perform tests in conformance with relevant Recommendations, may be provided within the clock generator and/or test sequence generator or it may be provided separately. In this Recommendation it is assumed that the modulation source is sinusoidal. However, random stimuli may be required for certain tests. Details need to be studied.

7.2 Clock generator

It shall be possible to phase modulate the clock generator from the modulation source and to indicate the peak-to-peak phase deviation of the modulated signal.

The generated peak-to-peak jitter and the modulating frequencies shall meet the minimum requirements of Figure 2 and Table 2.

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[2] In the case of 1544 kbit/s, the test signal source shall have the following return loss: 20 kHz to 500 kHz ≥ 14 dB and 500 kHz to 1.6 MHz ≥ 16 dB.

The modulating input sensitivity of the clock generator shall be at least:

1 volt peak-to-peak into 75 Ω for bit rates up to and including 139 264 kbit/s.

The minimum output of the modulated clock signal and the external timing reference signal shall be 1 volt peak-to-peak into 75 Ω.

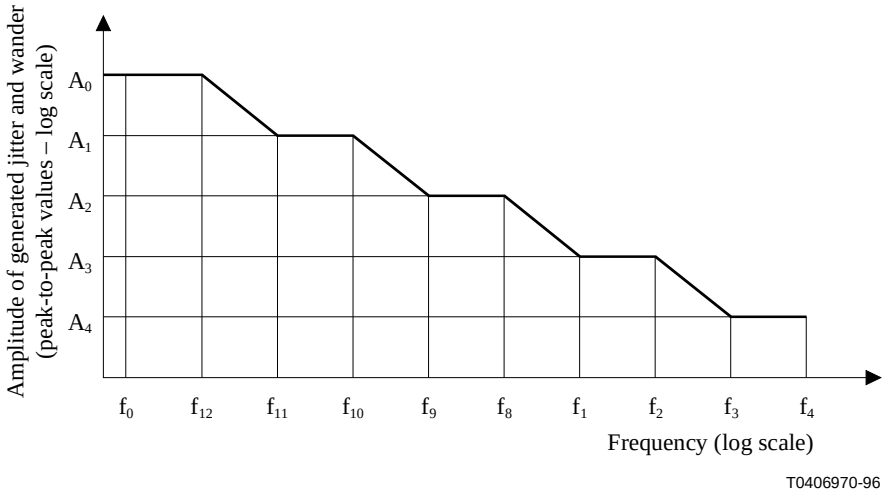

Figure 2/O.171 – Generated jitter amplitude versus jitter frequency

Table 2/O.171 – Minimum amplitude of adjustable generated jitter amplitude versus jitter frequency

Bit rate (kbit/s)	**A_0**	**A_1**	**A_2**	**A_3**	**A_4**	**f_0**	**f_{12}**	**f_{11}**	**f_{10}**	**f_9**	**f_8**	**f_1**	**f_2**	**f_3**	**f_4**
	in UI					**in Hz**									
64			a)	5	0.5				a)	a)	a)	2	600	6 k	20 k
1 544				10	0.5							2	400	8 k	40 k
2 048	40		20	10	0.5	12μ					5	10	900	18 k	100 k
6 312				10	0.5							2	1 600	32 k	60 k
8 448	200		20	10	0.5	12μ			a)	a)	10	20	400	8.5 k	400 k
32 064				10	0.5							2	1 600	32 k	400 k
34 368	1 000		20	10	0.5	a)			a)	a)	50	100	1 000	20 k	800 k
44 736				10	0.5							2	5 000	100 k	400 k
139 264	3 000		20	10	0.5	a)			a)	a)	50	100	500	10 k	3 500 k

a) Values under study in Recommendation G.823.

NOTE to Figure 2 and Table 2 – Jitter amplitudes are specified as peak-to-peak values in Unit Intervals (UI). Values are based on Table 2/G.823 and Figure 3/G.823 for the 2048 kbit/s hierarchy and on Table 2/G.824 and Figure 3/G.824 for the 1544 kbit/s hierarchy.

7.2.1 Accuracy of the clock generator

The deviation of the internal clock signal from the nominal value shall be less than 10^{-5}.

As an option, the clock generator may provide frequency offset of sufficient magnitude to facilitate testing across the equipment clock tolerance range, e.g. ±10 ppm to ±100 ppm, as defined for the various bit-rates in Recommendation G.703 [2].

7.3 Test sequence generator

The jitter measuring circuit will normally be used with any suitable test sequence generator providing the following facilities.

NOTE – When test signals are applied to the input of a digital demultiplexer, they shall contain the frame alignment signal and – for certain measurements – justification control bits.

7.3.1 Test sequences

The test sequence generator shall be capable of providing the following signals:

NOTE – Longer pseudo-random test sequences may be necessary for jitter measurements on digital line systems and digital line sections (see Annex A/G.823 [7]).

For use at bit rates of 64 kbit/s, a pseudo-random test sequence of $2^{11} – 1$ bit length corresponding to 5.2/O.150 [10]. Encoding in accordance with 1.2.1/G.703 [2].

For use at bit rates of 2048 kbit/s, 6312 kbit/s, 8448 kbit/s, 32 064 kbit/s and 44 736 kbit/s, a pseudo-random test sequence of $2^{15} – 1$ bit length corresponding to 5.3/O.150 [10].

For use at bit rates of 1544 kbit/s, 6312 kbit/s, 32 064 kbit/s and 44 736 kbit/s, a pseudo-random test sequence of $2^{20} – 1$ bit length corresponding to 5.5/O.150 [10].

For use at bit rates of 34 368 kbit/s and 139 264 kbit/s, a pseudo-random test sequence of $2^{23} – 1$ bit length corresponding to 5.6/O.150 [10].

For use at all PDH bit rates, a 1000 1000 repetitive test sequence.

As an option and for use at all PDH bit rates:

a) two freely programmable 8-bit test sequences capable of being alternated at a low rate (e.g. from 10 Hz to 100 Hz);

b) a freely programmable 16-bit test sequence.

7.3.2 Generation errors

The test signal source shall be compatible with the jitter measuring circuit in such a way that the overall measuring accuracy is not substantially deteriorated. The measuring accuracy may be increased by measuring the jitter applied to the unit under test using the jitter measuring device described below.

8 Jitter measuring circuit

8.1 Input sensitivity of the electrical interfaces

The jitter measuring circuit is required to operate satisfactorily under the following input conditions:

a) The specification for equipment output ports listed in Recommendation G.703 [2].

b) The jitter measuring circuit shall also be capable of measuring at protected test points as defined in Recommendation G.772 [3].

8.2 Jitter measurement ranges

8.2.1 Measurement of peak-to-peak jitter

The jitter measuring circuit shall be capable of measuring peak-to-peak jitter. The measurement ranges to be provided are optional, but for reasons of compatibility the jitter amplitude/jitter frequency response of the jitter measuring circuit shall meet the minimum requirements of Figure 3 and Table 3 where f_1 to f_4 are the frequencies defining the jitter frequencies to be measured.

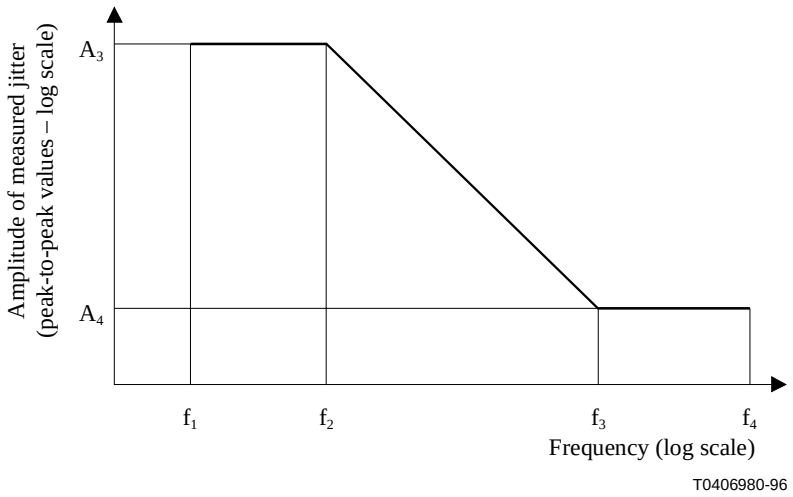

Figure 3/O.171 – Measured jitter amplitude versus jitter frequency

Table 3/O.171 – Minimum measured jitter amplitude versus jitter frequency

Bit rate (kbit/s)	A_3 in UI	A_4 in UI	f_1 in Hz	f_2 in Hz	f_3 in Hz	f_4 in Hz
64	5	0.5	20	600	6 k	20 k
1 544	10	0.5	10	400	8 k	40 k
2 048	10	0.5	20	900	18 k	100 k
6 312	10	0.5	10	1 600	32 k	60 k
8 448	10	0.5	20	400	8.5 k	400 k
32 064	10	0.5	10	1 600	32 k	400 k
34 368	10	0.5	100	1 000	20 k	800 k
44 736	10	0.5	10	5 000	100 k	400 k
139 264	10	0.5	200	500	10 k	3 500 k

8.2.2 Selectable threshold

When measuring peak-to-peak jitter, it shall also be possible to count the number of occasions and the period of time for which a given selectable threshold of jitter is exceeded. It shall be possible to record these events by means of an external counter, or an internal counter as an option.

It shall be possible to set the threshold at any selected measurement value within the measuring range of the jitter measuring circuit.

8.2.3 Measurement of r.m.s. jitter

Measurement of r.m.s. jitter may be performed using the analogue output mentioned in 8.5.1.

8.3 Measurement bandwidths

The basic jitter measuring circuit shall contain filters to limit the band of the jitter frequencies to be measured at the various bit rates. Additional filters shall be provided to further limit the bandwidth for the measurement of specified jitter spectra as defined in the G-Series Recommendations and for other uses. These additional filters may be either internal or external to the jitter measuring circuit. The filters are to be connected between the phase detector and the measuring device. The bandwidth of the jitter measuring circuit and the filters shall be in accordance with Table 4.

8.3.1 Frequency response of jitter measuring circuit and filters

The response of all filters within the passband shall be such that the accuracy requirements of the jitter measuring circuit are met.

At frequencies below the lower −3 dB point, the attenuation of the highpass filtration shall rise with a value equal to 20 dB per decade.

At frequencies above the upper −3 dB point, the attenuation of the lowpass filtration shall rise with a value greater than, or equal to, 60 dB per decade. However, the maximum attenuation of the filters shall be at least 60 dB. These filter requirements are in accordance with Recommendation G.823 [7]. For certain bit rates (1544, 6312, 32 064, 44 736 kbit/s), the attenuation of the lowpass filtration above the upper −3 dB point shall rise with a value equal to 20 dB per decade. These filter requirements are in accordance with Recommendation G.824 [8].

NOTE – Depending on the transient response of the filters, bursty jitter may affect the measuring accuracy.

Table 4/O.171 – Jitter measurement bandwidth and highpass filter cut off frequencies

Bit rate (kbit/s)	Jitter measurement bandwidth				3 dB point of the supplementary filters	
	f_0 (lower 3 dB point) (Hz)	f_1 (Hz)	f_4 (kHz)	f_5 (upper 3 dB point) (kHz)	Highpass filter No. 1	Highpass filter No. 2
64	2	20	20	≤ 40	20 Hz	3 kHz
1 544	2	10	40	≤ 80	10 Hz	8 kHz
2 048	2	20	100	≤ 200	20 Hz	18 kHz (0.7 kHz)
6 312	2	10	60	≤ 120	10 Hz	3 kHz
8 448	2	20	400	≤ 800	20 Hz	3 kHz (80 kHz)
32 064	2	10	400	≤ 800	10 Hz	8 kHz
34 368	2	100	800	≤ 1 600	100 Hz	10 kHz
44 736	2	10	400	≤ 800	10 Hz	30 kHz
139 264	2	200	3 500	≤ 7 000	200 Hz	10 kHz

NOTE 1 – The accuracy of the instrument is specified between frequencies f_1 and f_4.

NOTE 2 – Two values are specified for highpass filter No. 2 at 2048 kbit/s and 8448 kbit/s. The values shown in parenthesis only apply to measurements at certain national interfaces.

8.4 Measurement accuracy

8.4.1 General

The measuring accuracy of the jitter measuring circuit is dependent upon several factors such as fixed intrinsic error, frequency response and test sequence-depending error of the internal reference timing circuits. In addition there is an error which is a function of the actual reading.

The total error at 1 kHz jitter frequency (excluding the error due to frequency response) shall be less than:

$$\pm 5\% \text{ of reading} \pm X \pm Y$$

where X is the fixed error of Table 5 and Y an error of 0.01 UI p-p (0.002 UI_{rms}) which applies if internal timing extraction is used.

8.4.2 Fixed error

For the system bit rates and for the indicated test sequences, the fixed error of the jitter measuring circuit shall be as listed in Table 5 when measured at any jitter frequency between f_1 and f_4 of Figure 3.

8.4.3 Error at other frequencies

At jitter frequencies between f_1 and f_4 other than 1 kHz, the error additional to that defined in 8.4.1 above shall be as listed in Table 6.

Table 5/O.171 – Fixed error in jitter measurements

Bit rate (kbit/s)	Peak-to-peak jitter in UI for given test sequences		
	1000 1000	Pseudo-random[a)]	All ones or clock input
64	< 0.005	< 0.025	< 0.004
1 544	< 0.005	< 0.025	< 0.004
2 048	< 0.005	< 0.025	< 0.004
6 312	< 0.005	< 0.025	< 0.004
8 448	< 0.005	< 0.025	< 0.004
32 064	< 0.025	< 0.055	< 0.020
34 368	< 0.025	< 0.055	< 0.020
44 736	< 0.025	< 0.055	< 0.020
139 264	< 0.030	< 0.085	< 0.025

a) See 7.3.1.

NOTE – For bit rates above 32 Mbit/s, the values given in this Table need to be aligned with Recommendations G.823, G.824 and G.783. This requires further study.

Table 6/O.171 – Frequency response error

Bit rate (kbit/s)	Measurement bandwidth		Additional error referring to error at 1 kHz
	f_1 (Hz)	f_4 (kHz)	
64	20	20	± 2% 20 Hz to 600 Hz ± 3% 600 Hz to 10 kHz
1 544	10	40	± 4% f_1 to 1 kHz; ± 2 % to f_4
2 048	20	100	± 2% f_1 to f_4
6 312	10	60	± 4% f_1 to 1 kHz; ± 2 % to f_4
8 448	20	400	± 2% f_1 to 300 kHz ± 3% 300 kHz to f_4
32 064	10	400	± 2% 60 Hz to 300 kHz
34 368	100	800	± 3% 300 kHz to f_4
44 736	10	400	± 4% 10 Hz to 200 Hz ± 2% 200 Hz to 300 kHz
139 264	200	3 500	± 3% 300 kHz to 1 MHz ± 5% 1 MHz to 3 MHz ± 10% ≥ 3 MHz

8.4.4 Test sequence dependent error

The accuracy requirements stated above can be met when periodic test sequences with low zero content or clock signals are used to perform the jitter measurement. When using pseudo-random or random sequences or AMI and NRZ encoded signals, larger measurement errors have to be expected. Considering the bandwidths specified above, signals with higher zero content may even infringe the sampling theorem which – for theoretical reasons – makes it impossible to meet the accuracy requirements.

8.4.5 Pulse shape at the measurement access point

The accuracy requirements given in 8.4 apply to rectangular waveforms at the measurement access point. Non-rectangular waveforms may result in inter-symbol interference and may cause jitter measurement errors. This shall be taken into account, for example, when measuring at relevant interfaces of the 1544 kbit/s digital hierarchy.

8.5 Additional facilities

8.5.1 Analogue output

The jitter measuring circuit shall provide an analogue output signal to enable measurements to be made externally to the jitter measuring circuit, for example, by using an oscilloscope or an r.m.s. meter.

8.5.2 Reference timing signal

A reference timing signal for the phase detector is required. For end-to-end measurements of jitter, it may be derived in the jitter measuring circuit from any input test sequence. For loop-measurements, it may be derived from a suitable clock source.

9 Operating environment

The electrical performance requirements shall be met when operating at the climatic conditions as specified in 2.1/O.3 [9].

APPENDIX I

Guidelines concerning the measurement of jitter

Introduction

This Appendix contains tutorial information concerning the measurement of jitter. Various affects causing jitter are described in addition to different jitter measurement techniques. The jitter measurement configurations depicted in Figures I.1 to I.5 do not necessarily conform to practical test equipment implementations but are given in a general form for reasons of clarity. This should be taken into account when studying this Appendix.

I.1 Definitions and causes of jitter

Recommendation G.701 [1] defines *jitter* as "short-term non-cumulative variations of the significant instants of a digital signal from their ideal position in time". This means that jitter is an (unwanted) phase modulation of the digital signal. The frequency of the phase variations is called *jitter-frequency*. A second parameter which is closely related to jitter is called *wander*. It is defined as "long-term non-cumulative variations of the significant instants of a digital signal from their ideal

position in time". Up to now there is no clear definition of the boundary between jitter and wander. Components of phase variation having frequencies below the range of 1 to 10 Hz are normally called wander.

Jitter may deteriorate the transmission performance of a digital circuit. As a result of signal displacement from its ideal position in time, errors may be introduced into the digital bit stream at points of signal regeneration. Slips may be introduced into digital signals resulting from either data overflow or depletion in digital equipment incorporating buffer stores and phase comparators. In addition, phase modulation of the reconstructed samples in digital-to-analogue conversion devices may result in degradation of the decoded analogue signals. This is more likely to be a problem when transmitting encoded wide-band signals.

A distinction must be made between the *systematic* and *random* jitter. Systematic jitter results from misaligned timing recovery circuits in signal regenerating devices or from inter-symbol interference and amplitude-to-phase conversion caused by imperfect cable equalization. Systematic jitter is pattern-dependent.

Random jitter originates from internal or external interfering signals such as repeater noise, crosstalk or reflections. Random jitter is independent of the transmitted pattern.

Low-frequency jitter produced in pulse justification demultiplexers arises from pulse justification synchronization; the mechanism by which the plesiochronous lower-rate signals are synchronized to a locally generated clock source. This jitter, which appears at the demultiplexer lower-rate output, is denoted "justification jitter" or "waiting time jitter".

As systematic jitter is correlated with the transmitted pulse pattern at different regenerators, it accumulates coherently. Random jitter is uncorrelated at different regenerators and accumulates incoherently. In most lower-rate digital systems, systematic jitter is dominant. In higher-rate systems, the random component may become significant or even predominant.

Unlike some other impairments, disturbing jitter can be reduced by regenerators or by the use of "de-jitterizers" which contain a signal buffer with a narrow-band phase-smoothing circuit. Regenerators can only reduce jitter frequency components above the cut-off frequency of the clock recovery circuits. At lower jitter frequencies, the output signal or a regenerator follows the input jitter. In this case jitter is "transferred" which means that a regenerator behaves like a low-pass filter. This characteristic behaviour leads to the typical jitter tolerance templates as shown in Figure I.1.

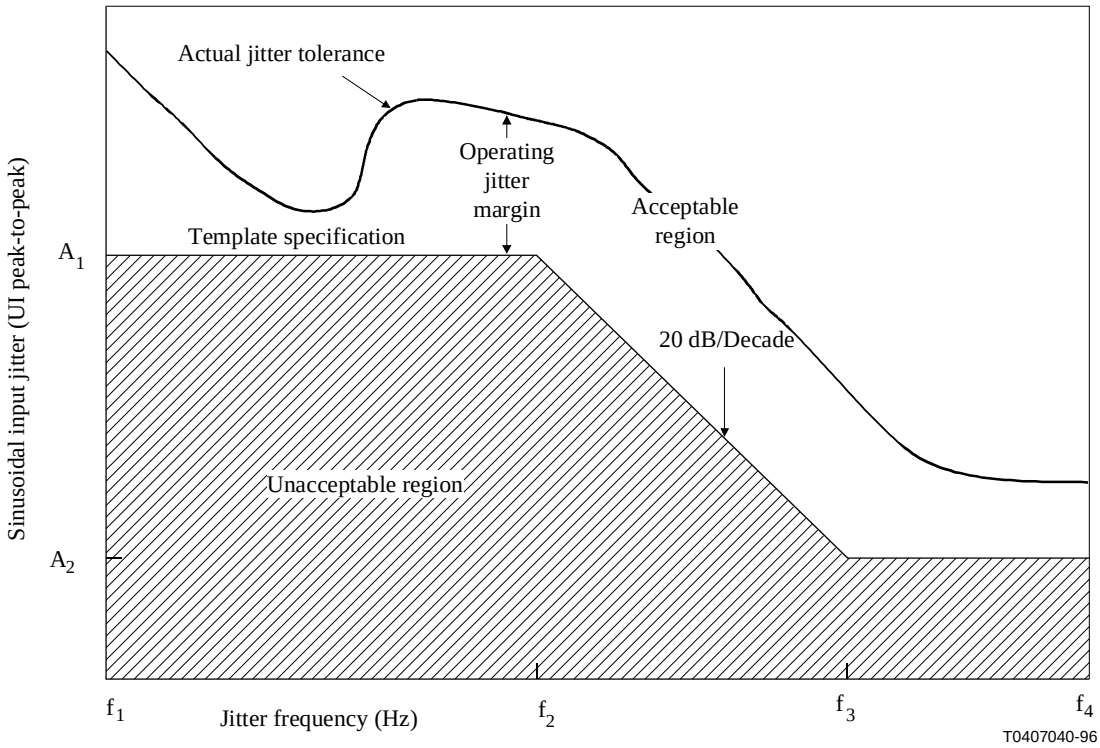

Figure I.1/O.171 – Actual tolerance measurement and tolerance template relationship

It can be seen from the considerations above that jitter can severely deteriorate the performance of digital transmission systems. On the other hand, jitter cannot be avoided completely. To evaluate whether jitter is kept within the allowed limits is the task of jitter measurements.

I.2 Test environment

In order to facilitate repeatable and accurate measurements, and to allow comparisons between measurements made at different times, it is necessary to minimize variations in the test environment. Several test environment parameters which may vary widely within their allowed ranges and may significantly affect jitter measurement results (depending upon the type of equipment involved) include the test sequence, bit rate, pulse shape, and cable characteristics. The characteristics of these parameters should be controlled as appropriate. Additionally, there are secondary test environment parameters which may also affect jitter performance, that should be maintained at nominal levels to facilitate repeatable measurements.

In order to verify worst-case equipment performance, it may be necessary to stress the equipment under test with multiple changes in the test environment. However, this type of test does not necessarily provide meaningful jitter performance data due to lack of control of the particular parameter(s) which may be causing errors, as well as their effect on other non-jitter related equipment failure mechanisms. Therefore, multiple changes in test environment should not be used to characterize the jitter performance of the equipment under test.

I.2.1 Controlled test sequences

Some measurement procedures require the application of controlled test sequences. When the controlled test sequence is intended to approximate live traffic encountered in the network, a Pseudo-Random Bit Sequence (PRBS) is recommended. For bit rates covered in Recommendations, four pseudo-random patterns are specified in Recommendation O.150, namely $2^{11} – 1$, $2^{15} – 1$, $2^{20} – 1$ and $2^{23} – 1$ length sequences. To ensure that a particular PRBS will generate adequate jitter spectral

line density within the jitter half-power bandwidth of typical clock recovery circuits at the applicable hierarchical level, the PRBS word length should be much greater than the bit rate divided by the jitter half-power bandwidth. The ITU-T recommends that the PRBS word length be at least 100 times greater than the bit rate divided by the jitter half-power bandwidth [7]. The pseudo-random bit sequence of $2^{15} - 1$ bit length specified in Recommendation O.150 for bit error measurements may generate an inadequate spectral line density for jitter measurements at bit rates above the primary rate. Moreover, this pattern has poor binary run properties. Therefore, for bit rates at and above the primary rate, the pattern length should be no less than $2^{20} - 1$, and have a well-balanced binary run characteristic [12].

I.2.2 Bit rate

The bit rate must be maintained within the specifications for digital interfaces as specified in Recommendation G.703 [2]. For convenience, the bit rates are repeated below:

– basic rate: 64 kbit/s ± 100 ppm;

– primary rate: 1 544 kbit/s ± 50 ppm;
2 048 kbit/s ± 50 ppm;

– secondary rate: 6 312 kbit/s ± 30 ppm;
8 448 kbit/s ± 30 ppm;

– tertiary rate: 32 064 kbit/s ± 10 ppm;
34 368 kbit/s ± 20 ppm;
44 736 kbit/s ± 20 ppm;

– quaternary rate: 139 264 kbit/s ± 15 ppm.

I.2.3 Pulse shape and cable characteristics

Pulse shape affects jitter performance by impacting the accuracy of the decision-making process in a block recovery circuit. Pulse shape is typically specified by a pulse template at an output interface or at a cross-connect [11] and may vary at the equipment input due to cable effects, resulting from operating within the specified range of cable lengths and specified cable type(s). It is recommended that the pulse shape to be used in jitter tests be centered within the pulse template specified, rather than being at the extreme allowable values (see Note).

NOTE – A pulse template appropriate for jitter testing needs further study.

I.2.4 Secondary test environment parameters

Other test environment parameters which may affect jitter performance include temperature, cross-talk, and noise. Temperature affects jitter performance by altering the resonant frequency of clock recovery circuits, oscillators, and phase-smoothing circuits, as well as changing the filtering properties of analog circuitry. Cross-talk may affect jitter performance when signals in a cable, backplane, or circuit board affect one another to a noticeable degree. Noise affects the decision-making process in a clock recovery circuit by decreasing the decision eye margin.

In order to obtain accurate and repeatable jitter measurements and ensure that the effects of jitter applied to the equipment dominate measurement results, it is recommended that these secondary parameters be maintained at their nominal levels.

I.3 Glossary of test configuration functional block components

This glossary defines the functional block components employed in the test configurations described in the following subclauses. Note that these functional blocks may be incorporated in various combinations within different test equipment.

– *Attenuator:* A device which reduces the amplitude of a digital signal in order to decrease the signal-to-noise ratio.

– *Test sequence:* A signal source which provides a digital network hierarchical signal at the appropriate bit rate with proper output impedance, pulse shape, line coding, and frame format. This functional block component is capable of providing several test sequences, must have a clock and data output, and may accept an external clock input.

– *Digital signal monitor:* An instrument which terminates a digital network hierarchical signal and monitors for bit errors, errored seconds, or Bit Error Ratio (BER).

– *Equipment Under Test (EUT):* A circuit or system that is being tested with a controlled test sequence.

– *Frequency synthesizer:* An extremely stable frequency source of high accuracy. Some frequency synthesizers are capable of adding Phase or Frequency Modulation (PM or FM) to the primary output while providing an unmodulated secondary output.

– *Jitter generator:* An instrument which produces a hierarchical rate clock modulated by sinusoidal jitter of adjustable frequency and amplitude. A modulation input provides for external jitter control, and an optional clock input provides for external bit rate frequency control.

– *Jitter measuring circuit:* A device which demodulates and measures the jitter present on a hierarchical clock or data signal or test sequence. An output provides a voltage proportional to the demodulated jitter.

– *Low-pass filter:* A circuit used to attenuate unwanted spectral components above a given frequency.

– *Jitter measurement filter:* A circuit which attenuates jitter spectral components outside a specified or desired passband.

– *Network under test:* A circuit, system, or network that is being tested using live traffic.

– *Noise source:* An instrument which generates a signal having a near Gaussian amplitude distribution with a flat power spectrum to approximately three times the half-power bandwidth of the timing recovery circuit of the EUT.

– *Modulation source:* A waveform generator which provides a low distortion frequency and amplitude controlled sine wave.

– *Spectrum analyzer:* An instrument which measures and displays signal power as a function of frequency over a selected frequency range. A tracking oscillator output provides an adjustable amplitude swept frequency sinusoid which tracks the instantaneous measurement frequency of the spectrum analyzer.

– *Voltmeter:* An instrument which measures DC, true r.m.s., or true peak-to-peak voltage as required. Here true peak-to-peak voltage is defined as the difference between the most positive and the most negative instantaneous voltages recorded during the entire measurement interval.

I.4 Jitter tolerance measurement

Jitter tolerance (also known as jitter accommodation) is defined in terms of the sinusoidal jitter amplitude which, when applied to an equipment input, causes a designated degradation of error performance. Jitter tolerance is a function of the amplitude and frequency of the applied jitter.

Jitter tolerance requirements are specified in terms of jitter templates which cover a specified sinusoidal amplitude/frequency region. Jitter templates represent the minimum amount of jitter an equipment *must accept* without causing the designated degradation of error performance (see Note).

The intended relationship of an equipment's actual tolerance to input jitter and its associated jitter tolerance template is illustrated in Figure I.1.

NOTE – In ITU-T terminology, the jitter tolerance template represents the "lower limit of maximum tolerable input jitter".

I.4.1 Actual tolerance

The sinusoidal jitter amplitudes that an equipment actually tolerates at a given frequency are defined as all amplitudes up to, but not including, that which causes the designated degradation of error performance.

The designated degradation of error performance may be expressed in terms of either Bit Error Ratio (BER) penalty or onset of errors criteria. The existence of two criteria arises because the input jitter tolerance of an individual digital equipment is primarily determined by the following two factors:

– The ability of the input clock recovery circuit to accurately recover clock from a jittered data signal, possibly in the presence of other degradations (pulse distortion, cross-talk, noise, etc.).

– The ability of other components to accommodate dynamically varying input bit rates (e.g. pulse justification capacity and synchronizer or desynchronizer buffer size in an asynchronous digital demultiplexer).

The BER penalty criterion allows environment independent determination of the decision circuit alignment jitter allocation, which is critical for evaluating the first factor. A detailed discussion of the BER penalty criterion may be found in References [13] and [14]. The onset of errors criterion is recommended for evaluating the second factor.

I.4.1.1 Bit error ratio penalty technique

The Bit Error Ratio (BER) penalty criterion for jitter tolerance measurements is defined as the amplitude of jitter, at a given jitter frequency, that duplicates the BER degradation caused by a specified Signal-to-Noise Ratio (SNR) reduction.

This technique is separated into two parts. Part one determines two BER versus SNR reference points for the equipment under test. With zero jitter applied, noise is added to the signal, or the signal is attenuated, until a convenient initial BER is obtained. Then the noise, or signal attenuation, is decreased until the SNR at the decision circuit is increased to the specified amount of dB (and consequently, the decision circuit is performing with an improved BER). Part two uses the BER versus SNR reference points; at a given frequency, jitter is added to the test signal until the BER returns to its initially selected value. Since a known decision circuit eye width margin was established by the two BER versus SNR points, the added equivalent jitter is a true and repeatable measure of the decision circuit jitter tolerance performance. Part two of the technique is repeated for a sufficient number of frequencies such that the measurement accurately represents the continuous sinusoidal input jitter tolerance of the EUT over the applicable frequency range. The test equipment must be able to produce a controlled jittered signal, a controlled SNR on the data stream, and measure the resulting BER from the EUT.

Figure I.2 illustrates the test configuration for the BER penalty technique. The equipment outlined in dashed lines is optional. The optional frequency synthesizer is used to provide a more accurate determination of frequencies utilized in the measurement procedure. This may be particularly important for repeatability of measurements for some types of equipment; i.e. asynchronous digital multiplexers. The optional jitter measuring circuit is used to verify the amplitude of generated jitter.

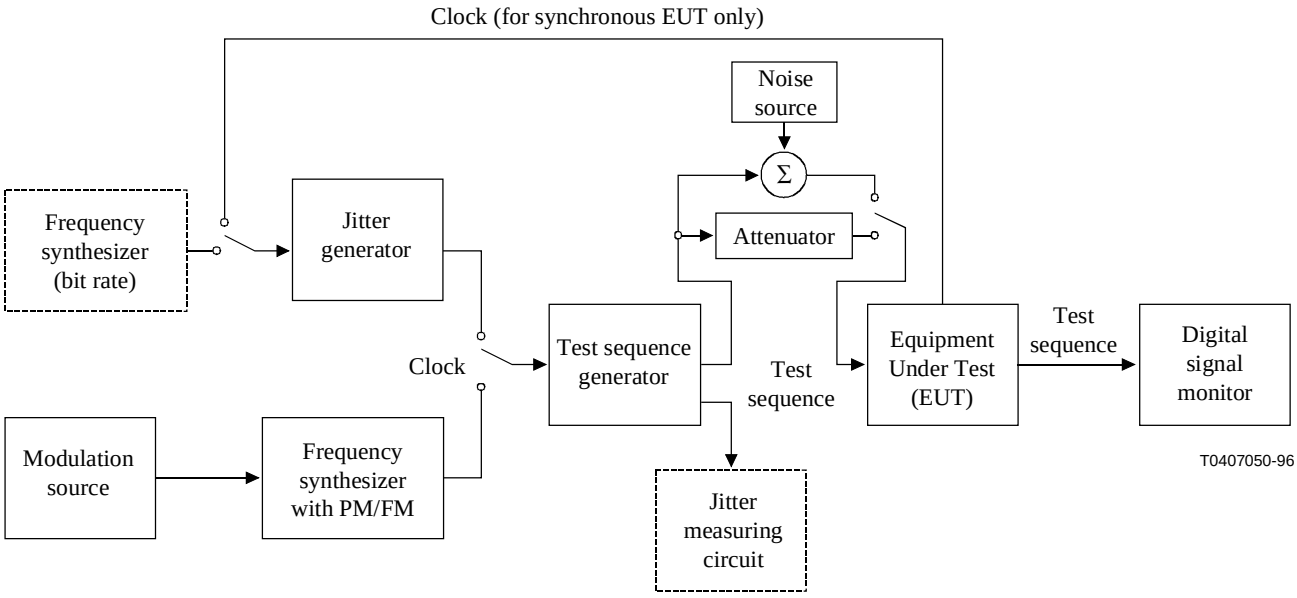

Figure I.2/O.171 – Jitter tolerance measurement configuration: Bit error ratio penalty technique

Procedure

i) Connect the equipment as shown in Figure I.2. Verify proper continuity and error-free operation.

ii) With no applied jitter, increase the noise (or attenuate the signal) until at least 100 bit errors per second are observed.

iii) Record the corresponding BER and its associated SNR.

iv) Increase the SNR by the specified amount.

v) Set the input jitter frequency as desired.

vi) Adjust the jitter amplitude until the BER returns to the value recorded in step iii).

vii) Record the amplitude and frequency of the applied input jitter, and repeat steps v) to vii) for a sufficient number of frequencies to characterize the jitter tolerance curve.

I.4.1.2 Onset of errors technique

The onset of errors criterion for jitter tolerance measurements is defined as the largest amplitude of jitter at a specified frequency that causes a cumulative total of more than 2 errored seconds, where these errored seconds have been summed over successive 30 seconds measurement intervals of increasing jitter amplitude.

This technique involves setting a jitter frequency and determining the jitter amplitude of the test signal which causes the onset of errors criterion to be satisfied. Specifically, this technique requires:

1) isolation of the jitter amplitude "transition region" (in which error-free operation ceases);
2) one errored second measurement, 30 seconds in duration, for each incrementally increased jitter amplitude from the beginning of this region; and
3) determination of the largest jitter amplitude for which the cumulative errored second count is no more than 2 errored seconds.

The process is repeated for a sufficient number of frequencies such that the measurement accurately represents the continuous sinusoidal input jitter tolerance of the EUT over the applicable jitter frequency range. The test equipment must be able to produce a controlled jittered signal and measure the resulting errored seconds caused by the jitter on the incoming signal.

Figure I.3 illustrates the test configuration for the onset of errors technique. The optional frequency synthesizer is used to provide a more accurate determination of frequencies utilized in the measurement procedure. The optional jitter measuring circuit is used to verify the amplitude of generated jitter.

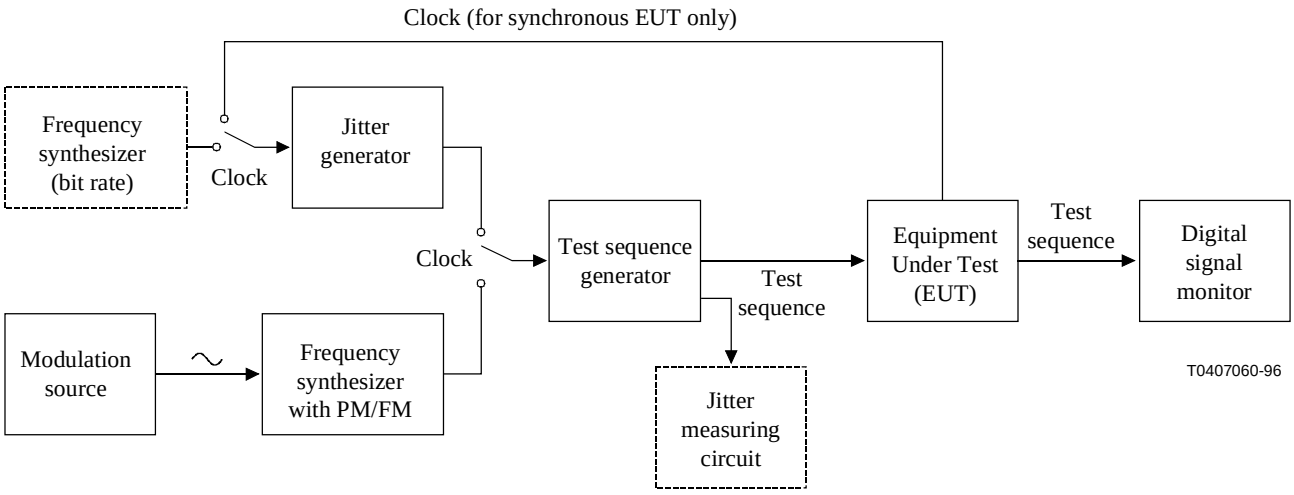

Figure I.3/O.171 – Jitter tolerance measurement configuration: Onset of errors technique

Procedure

i) Connect the equipment as shown in Figure I.3. Verify proper continuity and error-free operation.

ii) Set the input jitter frequency as desired, and initialize the jitter amplitude to 0 UI peak-to-peak.

iii) Increase the jitter amplitude in gross increments to determine the amplitude region where error-free operation ceases. Reduce the jitter amplitude to its level at the beginning of this region.

iv) Record the number of errored seconds that occur over a 30-second measurement interval. Note that the initial measurement must be 0 errored seconds.

v) Increase the jitter amplitude in fine increments, repeating step iv) for each increment, until the onset of errors criterion is satisfied.

vi) Record the indicated amplitude and frequency of the applied input jitter, and repeat steps ii) to iv) for a sufficient number of frequencies to characterize the jitter tolerance curve.

I.4.2 Jitter tolerance template compliance

Equipment jitter tolerance is specified with jitter tolerance templates. Each template defines the region over which the equipment must operate without suffering the designated degradation of error performance. The difference between the template and actual equipment tolerance curve represents the operating jitter margin, illustrated in Figure I.1.

The template compliance measurement is performed by setting the jitter frequency and amplitude to the template value, and observing that the designated degradation of error performance does not occur.

A sufficient number of template points are measured to assure compliance over the entire frequency range of the template.

Figure I.2 or I.3, as applicable, illustrates the test configuration for the jitter tolerance template compliance technique.

Procedure

i) Connect the equipment as described in I.4.1.1 or I.4.1.2, as applicable. Verify proper continuity and error-free operation.

ii) Set the jitter amplitude and frequency to a template point.

iii) When the onset of errors technique is used, confirm that 0 errored seconds occur. When the BER penalty technique is used, confirm that the designated degradation of error performance is not reached.

iv) Repeat steps ii) and iii) for a sufficient number of template points to verify jitter tolerance template compliance.

I.5 Jitter transfer characteristic measurement

The jitter transfer characteristic of an individual digital equipment is defined as the ratio of the output jitter to the applied input jitter as a function of frequency.

If the relationship between the jitter appearing at the input and output ports of a digital equipment can be described in terms of a linear process (a process which is both additive and homogeneous), the term "jitter transfer function" is used. The relationship between jitter appearing at the input and output ports of some types of digital equipment cannot be described in terms of a jitter transfer function. In such cases, different measurement techniques may be necessary to obtain meaningful results. Non-linear processes are not covered in this Appendix.

I.5.1 Linear processes

Jitter transfer measurements are commonly required for clock recovery circuits and desynchronizer phase smoothing circuits. Measurement of the jitter transfer function of a linear clock recovery circuit is generally straightforward. However, measurement of the jitter transfer function of a linear desynchronizer phase smoothing circuit requires specialized techniques because it is embedded in a non-linear asynchronous digital multiplexer.

I.5.1.1 Clock recovery circuit

Clock recovery circuits are an essential component of individual digital equipment input ports. Of particular interest is the jitter transfer function of clock recovery circuits which dominate the transfer of jitter from the input to output ports. Characterization of linear clock recovery circuits embedded in non-linear equipment (i.e. asynchronous digital multiplexers) are not addressed because they typically do not dominate the overall equipment jitter transfer characteristic.

I.5.1.1.1 Basic technique

This technique involves applying swept sinusoidal jitter at a fixed tolerable amplitude over a selected frequency range to the EUT, and observing the output jitter amplitude over the applied frequency range. The process is repeated for a sufficient number of frequency ranges to characterize the jitter transfer function of the EUT.

Specifically, this technique utilizes a spectrum analyzer to set a jitter frequency range and corresponding tolerable jitter amplitude. Initially, the EUT is bypassed to establish a 0 dB amplitude reference trace for the test equipment. The EUT is then re-connected, and the 0 dB amplitude reference trace subtracted from the overall jitter transfer measurement to obtain the EUT jitter transfer function. Use of a spectrum analyzer with a tracking oscillator output is required to determine the input jitter frequency and amplitude while making a narrow-band measurement of the output jitter. To achieve a high degree of accuracy, the spectrum analyzer bandwidth must be sufficiently narrow to obtain the desired amplitude resolution and dynamic range in each frequency band measured. For example, to verify less than 0.1 dB peaking, and a 20 dB per decade roll-off from 350 Hz to 20 kHz, a spectrum analyzer with 0.1 dB resolution, 3 Hz bandwidth, and 40 dB dynamic range may be required.

Figure I.4 illustrates the test configuration for the jitter transfer function measurement. The optional frequency synthesizer may be used to provide a more accurate determination of frequencies utilized in the measurement procedure.

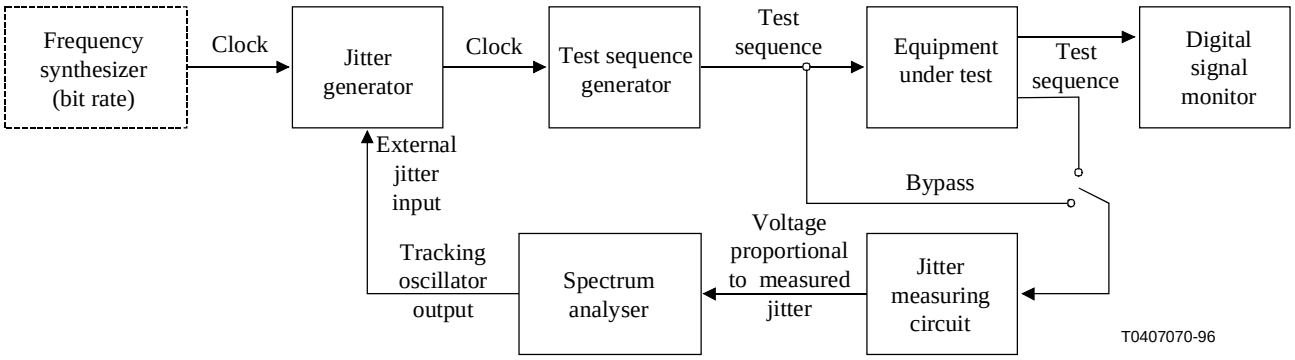

Figure I.4/O.171 – Jitter transfer function measurement configuration: Basic technique

Procedure

i) Perform a jitter tolerance measurement of the EUT over the desired frequency range, as described in I.4.

ii) Connect the equipment as shown in Figure I.4, bypassing the EUT. Verify proper continuity, linearity, and error-free operation.

iii) Set the frequency range on the spectrum analyzer as desired. Adjust the tracking oscillator output level on the spectrum analyzer to produce a tolerable jitter amplitude over the selected frequency range, which is large enough to ensure adequate measurement accuracy, yet sufficiently small to preserve linear operation.

iv) Set the spectrum analyzer bandwidth as narrow as feasible, sweep the desired frequency range, and record the 0 dB amplitude reference trace of the test equipment. (Setting a narrow spectrum analyzer bandwidth may allow a reduction in applied jitter amplitude with no loss in measurement accuracy.)

v) Re-connect the EUT as shown in Figure I.4. Verify proper continuity, linearity, and error-free operation.

vi) Use the spectrum analyzer to sweep the selected frequency range and record the magnitude of the overall (test equipment and EUT) jitter transfer function.

vii) To obtain the EUT jitter transfer function, subtract the 0 dB amplitude reference trace from the overall jitter transfer function recorded in step vi).

viii) Repeat steps i) to vii) for a sufficient number of frequency ranges to characterize the overall frequency range of interest.

I.5.1.2 Desynchronizer phase-smoothing circuit

In general, a non-linear process characterizes the relationship between the jitter appearing at the input and output ports of an asynchronous digital multiplexer. However, most phase-smoothing circuits are intended to operate linearly, and therefore may have a transfer function associated with them. Two techniques have been developed which enable the determination of the jitter transfer function for a linear desynchronizer phase-smoothing circuit using standard multiplex interfaces. The first technique utilizes interfaces at the multiplexer low bit rate input and the demultiplexer low bit rate output. The second technique utilizes the interfaces at the demultiplexer high bit rate input and low bit rate output. The second technique utilizes the interfaces at the demultiplexer high bit rate input and low bit rate output.

I.5.1.2.1 Multiplexer technique

This technique attempts to "linearize" the multiplexing process by applying appropriate constraints to the applied input jitter amplitude and frequency. Sinusoidal jitter of a selected amplitude and frequency is applied to the multiplexer low bit rate input, and the jitter amplitude at the demultiplexer low bit rate output is observed at the applied frequency. The process is repeated for a sufficient number of frequencies to characterize the desynchronizer jitter transfer function. Specifically, when sinusoidal jitter modulates the phase of the input signal to one of the multiplexer low bit rate inputs, the jitter spectrum appearing at the corresponding tributary outputs, in addition to containing other waiting time jitter components at discrete locations throughout the spectrum, contains a discrete component at the frequency of the input jitter. This technique involves making the amplitude of the input jitter sufficiently large to ensure that this discrete component in the output jitter spectrum at the applied frequency dominates the other waiting time jitter components in the measurement bandwidth. However, it should not be so large as to saturate the multiplexer stuffing mechanism (onset of saturation). The smallest magnitude of frequency deviation, $f(t)$, which causes onset of saturation is determined from the smaller magnitude of:

$$f(t) = f_{sc} - f_{nom}$$

$$f(t) = -f_m + f_{sc} - f_{nom}$$

where:

f_{sc} represents the multiplexer average synchronous data bit read clock rate;

f_m represents the maximum rate at which pulses can be stuffed into an incoming pulse stream,

and:

f_{nom} refers to the nominal incoming line rate.

To achieve a high degree of accuracy, the spectrum analyzer bandwidth must be sufficiently narrow to obtain the desired amplitude resolution and dynamic range in each frequency band measured (see I.5.1.1.1). It is also assumed that the transfer function of the multiplexer low bit rate input clock recovery circuit does not alter the applied jitter in the frequency range of interest.

Figure I.4 illustrates the test configuration for the jitter transfer function measurement. The optional frequency synthesizer may be used to provide a more accurate determination of frequencies utilized in the measurement procedure.

Procedure

i) Perform a jitter tolerance measurement over the desired frequency range.

ii) Connect the equipment as shown in Figure I.4, bypassing the EUT. Verify proper continuity, linearity, and error-free operation.

iii) Manually set the test frequency on the spectrum analyzer.

iv) Adjust the tracking oscillator output level on the spectrum analyzer to produce the largest tolerable jitter amplitude which will not cause onset of saturation (as defined in this subclause) at the selected frequency.

v) Set the spectrum analyzer bandwidth as narrow as feasible, and record the 0 dB amplitude transfer reference level of the test equipment.

vi) Reconnect the EUT as shown in Figure I.4. Verify proper continuity and error-free operation.

vii) Record the magnitude of the overall (test equipment and EUT) jitter transfer function. Averaging is generally required to remove the effects of waiting time jitter on the measurement.

viii) To obtain the magnitude of the EUT jitter transfer function, subtract the 0 dB amplitude transfer reference level from the overall magnitude obtained in step vii).

ix) Repeat steps iii) to viii) for a sufficient number of frequencies to characterize the jitter transfer function of the EUT.

I.5.1.2.2 Demultiplexer technique

This technique involves applying sinusoidal jitter of a selected amplitude and frequency to the demultiplexer high bit rate input, and observing the jitter amplitude at the demultiplexer low bit rate output at the applied frequency. The process is repeated for a sufficient number of frequencies to characterize the desynchronizer jitter transfer function. Specifically, when sinusoidal jitter modulates the phase of the input signal to the demultiplexer, the output jitter spectrum contains a discrete component at the frequency of the input jitter, in addition to the intrinsic waiting time jitter components already present. This technique involves making the amplitude of the applied input jitter sufficiently large to ensure that its contribution to the output jitter spectrum at the applied frequency dominates that of the waiting time jitter, but does not exceed the demultiplexer input jitter tolerance. It is also assumed that the transfer function of the demultiplexer high bit rate input clock recovery circuit does not alter the applied jitter in the frequency range of interest.

Figure I.4 illustrates the test configuration for the jitter transfer function measurement. It should be emphasized that the following procedure *cannot calibrate out the effects of the low bit rate receive circuitry contained in the jitter measuring circuit functional block component*, and therefore requires that this circuitry has flat response.

It should be noted that the digital signal applied to the high bit rate input of the demultiplexer must contain framing information to allow proper operation of the equipment under test. "Framed" signals can either be taken from an appropriate test sequence generator or may come from the corresponding

digital multiplexer. In the latter case, a transparent jitter modulator has to be inserted between the high-speed multiplexer output and the demultiplexer input. The jitter modulator superimposes jitter on the jitter-free signal coming from the multiplexer.

Procedure

– Follow the procedure provided in I.5.1.1.1 using Figure I.4, scaling the applied jitter in Unit Intervals (UIs) by the ratio of the demultiplexer high bit rate input to low-speed output bit rates.

I.6 Output jitter measurement

Output jitter measurements fall within two categories:

1) network output jitter at hierarchical interfaces; and

2) intrinsic jitter generated by individual digital equipment.

Measurements of output jitter may be in terms of r.m.s. and peak-to-peak amplitudes over designated frequency ranges, and may require statistical characterization.

Output jitter measurements utilize either live traffic or controlled test sequences.

I.6.1 Live traffic

Output jitter measurements at network hierarchical interfaces typically use a live traffic signal. For pre-service testing, in which controlled test sequences are used, see I.6.2. This technique involves demodulating the jitter from the live traffic at the output of a network interface, selectively filtering the jitter, and measuring the true r.m.s. or true peak-to-peak amplitude of the jitter over the specified measurement time interval.

Figure I.5 illustrates the test configuration for the live traffic technique. The optional spectrum analyzer allows observation of the output jitter frequency spectrum.

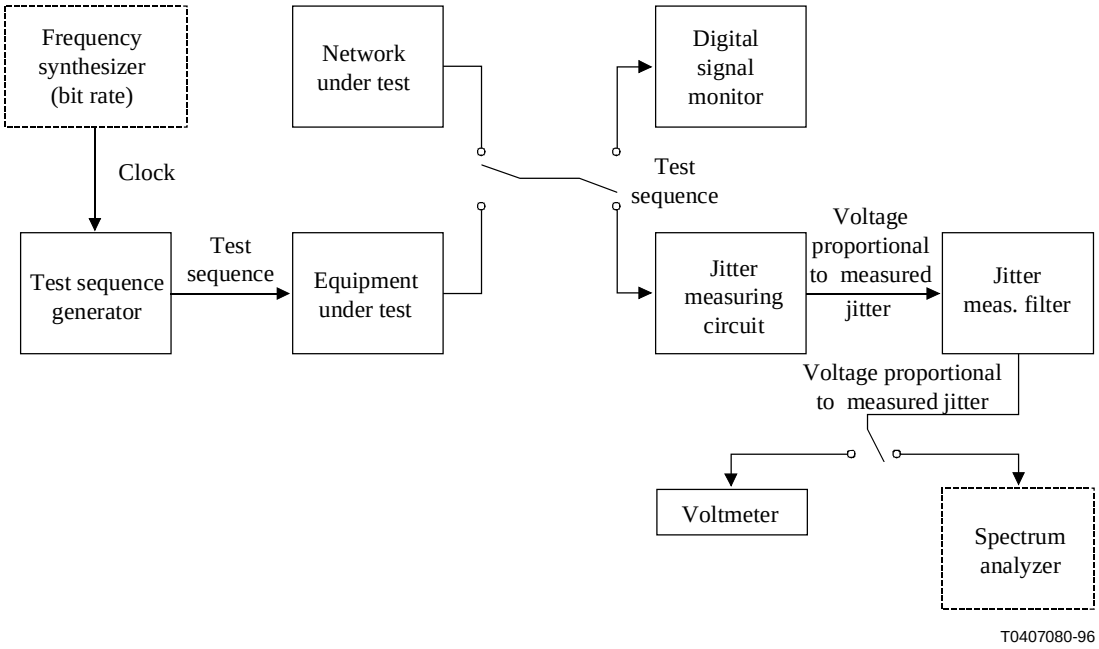

Figure I.5/O.171 – Output jitter measurement configuration: Basic technique

Procedure

i) Connect the equipment as shown in Figure I.5. Verify proper continuity and error-free operation.

ii) Select the desired jitter measurement filter and measure the filtered output jitter, recording the true peak-to-peak jitter amplitude that occurs during the specified measurement time interval.

iii) Repeat step ii) for all desired jitter measurement filters.

I.6.2 Controlled test sequences

Measurement of intrinsic jitter in individual digital equipment requires the application of controlled test sequences. Controlled test sequences are generally applicable in laboratory, factory, and out-of-service situations. The "basic technique", described below, details how such measurements may be performed.

Where it is desirable to obtain more detailed information regarding output jitter power (specifically, jitter generated in digital regenerators), jitter may be further categorized in terms of random and systematic components. The primary reasons for distinguishing between random and systematic jitter are to enable the comparison of measurement results with theoretical computations, and to refine regenerator design. The "enhanced technique" covered in Reference [13] describes how random and systematic jitter may be measured.

I.6.2.1 Basic technique

This technique is identical to that described in I.6.1, except for the application of an unjittered controlled test sequence to the EUT. In Figure I.5, the optional frequency synthesizer may be used to provide a more accurate determination of frequencies utilized in the measurement procedure.

Procedure

i) Connect the equipment as shown in Figure I.5, using the digital signal generator to provide an unjittered controlled test sequence to the EUT. Verify proper continuity and error-free operation.

ii) Select the desired jitter measurement filter and measure the filtered output jitter, recording the true peak-to-peak jitter amplitude that occurs during the specified measurement time interval.

iii) Repeat step ii) for all desired jitter measurement filters.

APPENDIX II

Guidelines concerning the measurement of wander

(This Appendix contains tutorial information only)

This edition of Recommendation O.171 only contains general information concerning the measurement of wander. Therefore, the relevant text has been placed into an Appendix. Measurement of wander will be studied further and may be included in the main body of future editions of Recommendation O.171.

II.1 Wander measurements

II.1.1 Wander measurement configurations – General considerations

Because of the low frequency of the phase variations to be evaluated (see definition in clause 3), wander is a quantity which requires a special test configuration. When performing jitter measurements, the required reference timing signal is normally produced locally. By means of a phase-locked loop, it is derived from the average phase of the signal to be measured. Such a phase-locked loop cannot be realized to cope with the requirements of wander measurements.

Therefore, wander measurements always require an external reference signal of adequate stability.

This subclause as well as II.1.2 and II.1.3 contain information on test configurations for wander measurements which are in accordance with Recommendation G.810 [4].

II.1.2 Synchronized wander measurements

Figure II.1 shows in a very general form the block diagram of circuit required for the synchronized measurement of wander.

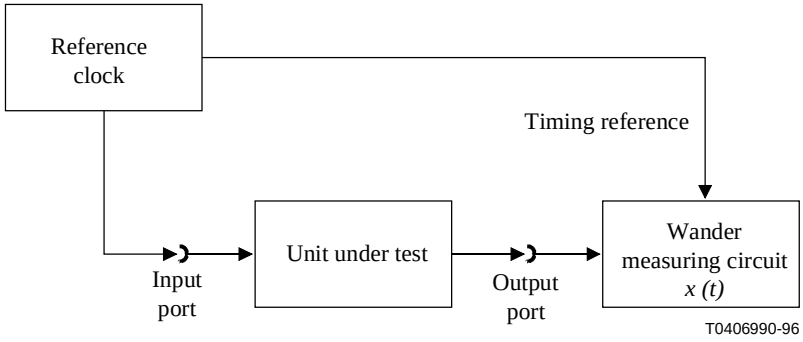

Figure II.1/O.171 – Synchronized wander measurement configuration

This configuration is applicable if the timing signals required to perform the measurement can be derived from a common reference clock. This means that only loop measurements – where input and output port of the unit under test are accessible at the same location – can be carried out this way. In this set-up, the measurement result is not affected by phase variations of the reference clock. Thus, the requirements on the stability of the reference clock are not very high and are achievable in portable test instrumentation.

II.1.3 Non-synchronized wander measurements

The block diagram for non-synchronized wander measurements is depicted in Figure II.2.

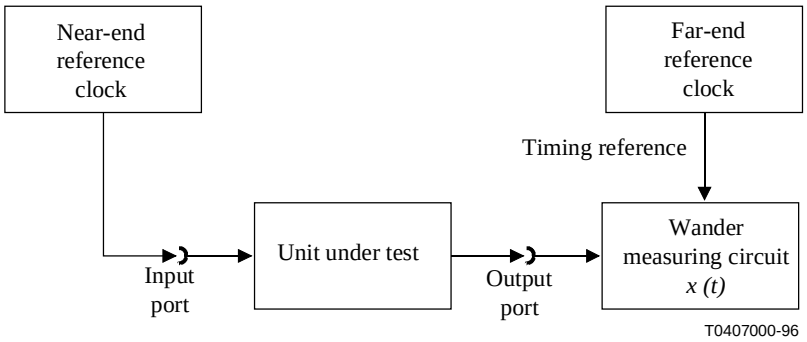

Figure II.2/O.171 – Non-synchronized wander measurement configuration

This configuration is applicable to wander measurements in cases where the input and output ports of the unit under test are not available at the same location (end-to-end measurements). In this set-up, the measurement result is affected by any frequency/phase drift of the two clocks involved in the measurement. This means that the stability of the two clocks has to be at least one order of magnitude better than the quantity to be measured. Such reference clocks may not be provided in portable test instrumentation but synchronization to an external reference is required.

II.2 Clock stability measurements

If the stability of a clock is to be measured, the measurement set-up is similar to that described above. It is illustrated in Figure II.3.

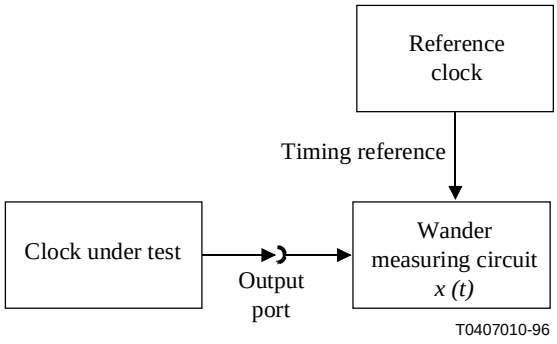

Figure II.3/O.171 – Clock stability measurement configuration

Also in this configuration, the measurement result is affected by any frequency/phase drift of the reference clock involved in the measurement. The same considerations as to Figure II.2 apply.

II.3 Quantities to be measured

The following wander quantities shall be measured:

II.3.1 Time deviation

The instrumentation shall be capable of measuring Time Deviation (TDEV) as defined in Recommendation G.810 [4].

II.3.2 Maximum time interval error

The instrumentation shall be capable of measuring the Maximum Time Interval Error (MTIE) as defined in Recommendation G.810 [4].

II.3.3 Allan deviation

The instrumentation may be capable of measuring Allan Deviation (ADEV) as defined in Recommendation G.810 [4].

II.4 External reference

Especially for the measurement of wander an input for an external reference signal is required. This input shall accept clock signals of the bit rate of 1544 kbit/s or 2048 kbit/s and sinusoidal signals at 1544 kHz or 2048 kHz as a reference.

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