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Digital sections and digital line system – Access networks

Single-pair high-speed digital subscriber line (SHDSL) transceivers – For approval – Updated

CAUTION !

PREPUBLISHED RECOMMENDATION

This prepublication is an unedited version of a recently approved Recommendation. It will be replaced by the published version after editing. Therefore, there will be differences between this prepublication and the published version.

FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

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NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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RECOMMENDATION G.991.2

SINGLE-PAIR HIGH-SPEED DIGITAL SUBSCRIBER LINE (SHDSL) TRANSCEIVERS - FOR APPROVAL - UPDATED

Abstract

Recommendation G.991.2 describes a transmission method for data transport in telecommunications access networks. SHDSL transceivers are designed primarily for duplex operation over mixed gauge two-wire twisted metallic pairs. Optional four-wire operation is supported for extended reach applications. Optional signal regenerators for both single-pair and two-pair operation are specified, as well. SHDSL transceivers are capable of supporting selected symmetric user data rates in the range of 192 kbit/s to 2 312 kbit/s using a Trellis Coded Pulse Amplitude Modulation (TC-PAM) line code. They are designed to be spectrally compatible with other transmission technologies deployed in the access network, including other DSL technologies. SHDSL transceivers do not support the use of analogue splitting technology for coexistence with either POTS or ISDN. Regional requirements, including both operational differences and performance requirements, are specified in Annexes A, B and C. Requirements for signal regenerators are specified in Annex D. Annex E describes application-specific framing modes that may be supported by SHDSL transceivers.

Summary

Recommendation G.991.2 describes a transmission method for data transport in telecommunications access networks. SHDSL transceivers are designed primarily for duplex operation over mixed gauge two-wire twisted metallic pairs. Optional four-wire operation is supported for extended reach applications. Optional signal regenerators for both single-pair and two-pair operation are specified, as well. SHDSL transceivers are capable of supporting selected

symmetric user data rates in the range of 192 kbit/s to 2 312 kbit/s using a Trellis Coded Pulse Amplitude Modulation (TC-PAM) line code. They are designed to be spectrally compatible with other transmission technologies deployed in the access network, including other DSL technologies. SHDSL transceivers do not support the use of analogue splitting technology for coexistence with either POTS or ISDN. Regional requirements, including both operational differences and performance requirements, are specified in Annexes A, B and C. Requirements for signal regenerators are specified in Annex D. Annex E describes application-specific framing modes that may be supported by SHDSL transceivers.

See G.992.1, Annex H [1] for specifications of transceivers for use in networks with existing TCM-ISDN service (as specified in G.961, Appendix III [B1]).

CONTENTS

1 Scope

This Recommendation describes a transmission method for providing Single-pair High-speed Digital Subscriber Line (SHDSL) service as a means for data transport in telecommunications access networks. This Recommendation does not specify all the requirements for the implementation of SHDSL transceivers. Rather, it serves only to describe the functionality needed to assure interoperability of equipment from various manufacturers. The definitions of physical user interfaces and other implementation-specific characteristics are beyond the scope of this Recommendation.

For interrelationships of this Recommendation with other G.99x-series Recommendations, see Recommendation G.995.1 [B2] (informative).

The principal characteristics of this Recommendation are as follows:

– provisions for duplex operation over mixed gauge two-wire or optional four-wire twisted metallic pairs;

– specification of the physical layer functionality, e.g. line codes and forward error correction;

– specification of the data link layer functionality, e.g. frame synchronization and framing of application, as well as Operations, Administration and Maintenance (OAM) data;

– provisions for optional use of repeaters for extended reach;

– provisions for spectral compatibility with other transmission technologies deployed in the access network;

– provisions for regional requirements, including functional differences and performance requirements.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

[1] ITU-T Recommendation G.992.1 (1999) - Asymmetric Digital Subscriber Line (ADSL) Transceivers.

[2] ITU-T Recommendation G.994.1 (2000) - Handshake procedures for Digital Subscriber Line (DSL) Transceivers.

[3] ITU-T Recommendation G.997.1 (1999) - Physical Layer Management for Digital Subscriber Line (DSL) Transceivers.

[4] IETF RFC 1662 - PPP in HDLC-like Framing.

[5] ISO 8601:1988 - Data elements and interchange formats - Information interchange - Representation of dates and times.

[6] ITU-T Recommendation G.996.1 (2000) - Test procedures for Digital Subscriber Line (DSL) Transceivers.

[7] IEC 60 950 - Safety of information technology equipment including electrical business equipment.

[8] ITU-T Recommendation I.432.1 (1999) - B-ISDN User-Network Interface - Physical Layer Specification: General Characteristics.

3 Definitions and abbreviations

3.1 Definitions

bit-error ratio	the ratio of the number of bits in error to the number of bits sent over a period of time.
downstream	STU-C to STU-R direction (central office to remote terminal).
loopback	a reversal in the direction of the payload (i.e. the user data) at a specified SHDSL network element.
mapper	a device for associating a grouping of bits with a transmission symbol.
micro-interruption	a temporary line interruption.
modulo	a device having limited value outputs (not the same as the mathematical modulo operation).
payload block	one of the sections of a frame containing user data.
plesiochronous	a clocking scheme in which the SHDSL frame is based on the input transmit clock but the symbol clock is based on another independent clock source.
precoder	a device in the transmitter for equalizing some of the channel impairments.
precoder coefficients	coefficients of the filter in the precoder that are generated in the receiver and transferred to the transmitter.
remote terminal	a terminal located downstream from a central office switching system.
scrambler	a device to randomize a data stream.
segment	the portion of a span between two terminations (either STUs or SRUs).
SHDSL network element	an STU-R, STU-C or SRU.
span	the link between STU-C and STU-R, including regenerators.
spectral shaper	a device that reshapes the frequency characteristics of a signal.
stuff bits	bits added to synchronize independent data streams.
synchronous	a clocking scheme in which the SHDSL frame and symbol clocks are based on the STU-C input transmit clock or a related network timing source.
upstream	STU-R to STU-C direction (remote terminal to central office).

3.2 Abbreviations

α	the interface between the PMS-TC and TPS-TC layers in an STU-C
β	the interface between the PMS-TC and TPS-TC layers in an STU-R
γ_C	the interface between the TPS-TC layer and the application specific section in an STU-C
γ_R	the interface between the TPS-TC layer and the application specific section in an STU-R
a_k	Convolutional Encoder Coefficients
AFE	Analogue Front End
AGC	Automatic Gain Control
b_k	Convolutional Encoder Coefficients
BER	Bit Error Ratio
bit/s	Bits Per Second
C_k	The kth Precoder Coefficient
CMRR	Common Mode Rejection Ratio
CO	Central Office
CPE	Customer Premise Equipment
CRC	Cyclic Redundancy Check
CRC6	CRC of Order 6 (used in SHDSL frame)
crc(X)	CRC Check Polynomial
DAC	Digital-to-Analogue Converter
dBm	dB reference to 1 mW, i.e. 0 dBm = 1 mW
DC	Direct Current
DLL	Digital Local Line
DS	Downstream
DSL	Digital Subscriber Line
DUT	Device Under Test
EOC	Embedded Operations Channel
ES	Errored Second
f_s	Sampling rate
f_{sym}	Symbol rate
FCS	Frame Check Sequence
FEC	Forward Error Correction
FEXT	Far-End Cross-Talk
FSW	Frame Synchronization Word
g(X)	Generating Polynomial for CRC

HDLC	High-level Data Link Control
HW	Hardware
I/F	Interface
kbit/s	Kilobits per second
LB	Longitudinal Balance
LCL	Longitudinal Conversion Loss
losd	Bit indicating Loss of signal at the application interface
LOSW	Loss Of Sync Word failure
LSB	Least Significant Bit
LT	Line Termination
m(X)	Message Polynomial for CRC
Mbit/s	Megabits per second
MSB	Most Significant Bit
MTU	Maintenance Termination Unit
NEXT	Near-End Cross-Talk
NT	Network Termination
OAM	Operations, Administration and Maintenance
OH	Overhead
PAM	Pulse Amplitude Modulation
2-PAM	PAM having two levels (used at startup)
PBO	Power Back-Off
PL-OAM	Physical Layer - OAM
PMD	Physical Media Dependent
PMMS	Power Measurement Modulation Session (Line Probe)
PMS-TC	Physical Media-Specific TC Layer
ppm	Parts Per Million
PPP	Point-to-Point Protocol
ps	Power status bit
PSD	Power Spectral Density
PTD	Path Terminating Device (CO side terminating equipment)
REG	Signal Regenerator
rms	Root mean square
RSP	Regenerator Silent Period bit
RX	Receiver
S/T	Logical interface between the STU-R and attached user terminal equipment

sb	stuff bit
sbid	stuff bit identified indicator bit
sega	segment anomaly indicator bit
segd	segment defect indicator bit
SES	Severely Errored Second
SHDSL	Single-Pair High-bit-rate DSL
SNR	Signal-to-Noise Ratio
SRU	SHDSL Regenerator Unit
STU	SHDSL Transceiver Unit
STU-C	STU at the Central Office
STU-R	STU at the Remote End
TBD	To Be Determined
TC	Transmission Convergence layer
TCM	Trellis Coded Modulation
TCM-ISDN	Time-Compression Multiplexed ISDN (specified in G.961, Appendix III [B1])
TCPAM	Trellis Coded PAM (used in data mode)
TPS-TC	Transmission Protocol-Specific TC Layer
TX	Transmitter
U-C	Loop Interface - Central Office end
U-R	Loop Interface - Remote Terminal end
UAS	Unavailable Second
US	Upstream
UTC	Unable to Comply
V	Logical interface between STU-C and a digital network element such as one or more switching systems
xDSL	a collective term referring to any of the various types of DSL technologies

4 Reference Models

4.1 STU-x Functional Model

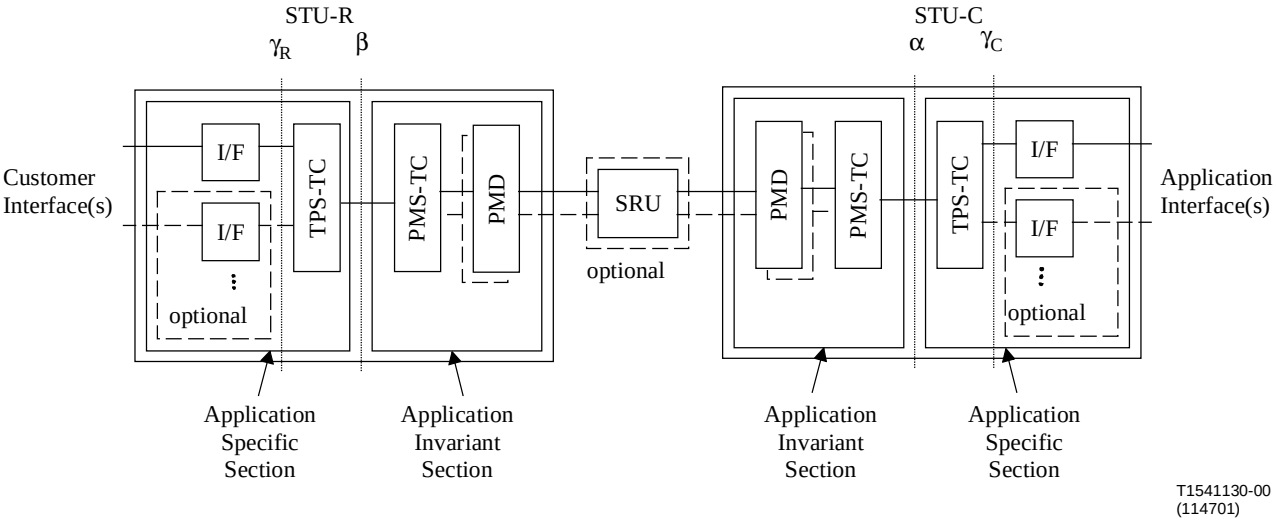


FIGURE 4-1

STU-x Functional Model

Figure 4-1 is a block diagram of an SHDSL Transceiver Unit (STU) transmitter showing the functional blocks and interfaces that are referenced in this Recommendation. It illustrates the basic functionality of the STU-R and the STU-C. Each STU contains both an application invariant section and an application specific section. The application invariant section consists of the PMD and PMS-TC layers, while the application specific aspects are confined to the TPS-TC layer and device interfaces. As shown in the figure, one or more optional signal regenerators may also be included in an SHDSL span. Management functions, which are typically controlled by the operator's network management system, are not shown in the figure. See § 9 for details on management. Remote power feeding, which is optionally provided across the span by the STU-C, is not illustrated in the figure.

The functions at the central office side constitute the STU-C (or Line Termination (LT)). The STU-C acts as the master both to the customer side functions of the STU-R (or Network Termination (NT)) and to any regenerators.

The STU-C and STU-R, along with the DLL (Digital Local Line) and any regenerators, make up an SHDSL span. The DLL may consist of a single copper twisted pair, or, in optional configurations, two copper twisted pairs. In the two-pair cases, each STU contains two separate PMD layers, interfacing to a common PMS-TC layer. If enhanced transmission range is required, one or more signal regenerators may be inserted into the loop at intermediate points. These points shall be chosen to meet applicable criteria for insertion loss and loop transmission characteristics.

The principal functions of the PMD layer are:

- symbol timing generation and recovery;
- coding and decoding;
- modulation and demodulation;

- echo cancellation;
- line equalization;
- link startup.

The PMD layer functionality is described in detail in § 6.

The PMS-TC layer contains the framing and frame synchronization functions, as well as the scrambler and descrambler. The PMS-TC layer is described in § 7.

The PMS-TC is connected across the α and β interfaces in the STU-C and the STU-R, respectively, to the TPS-TC layer. The TPS-TC is application specific and consists largely of the packaging of user data within the SHDSL frame. See § 8 for details. This may include multiplexing, demultiplexing, and timing alignment of multiple user data channels. Supported TPS-TC user data framing formats are described in Annex E.

The TPS-TC layer communicates with the Interface blocks across the γ_R and γ_C interfaces. Depending upon the specific application, the TPS-TC layer may be required to support one or more channels of user data and associated interfaces. The definition of these interfaces is beyond the scope of this Recommendation.

Note that the α, β, γ_R and γ_C interfaces are only intended as logical separations and need not be physically accessible.

4.2 User Plane Protocol Reference Model

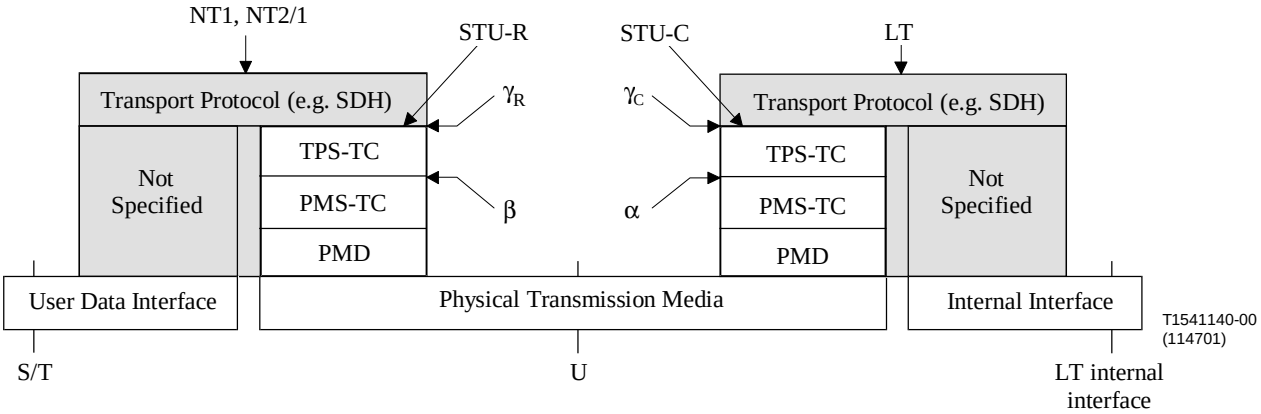


FIGURE 4-2

User Plane Protocol Reference Model

The User Plane Protocol Reference Model, shown in Figure 4-2, is an alternate representation of the information shown in Figure 4-1. This figure is included to emphasize the layered nature of this Recommendation and to provide a view that is consistent with the generic xDSL models shown in G.995.1 [B2].

4.3 Application Models

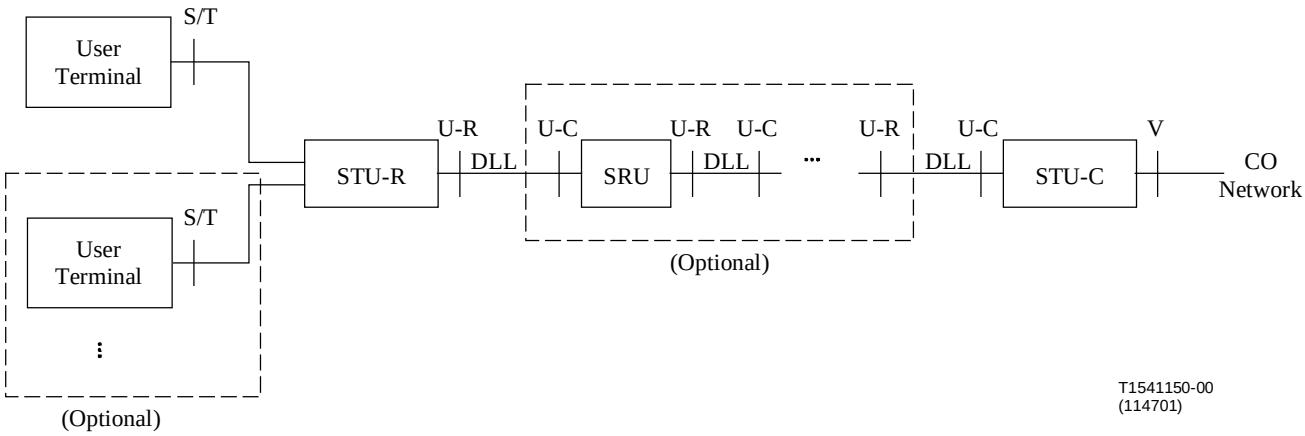


FIGURE 4-3

Application Model

Figure 4-3 is an application model for a typical SHDSL system, showing reference points and attached equipment. In such an application, an STU-R will typically connect to one or more user terminals, which may include data terminals, telecommunications equipment, or other devices. These connections to these pieces of terminal equipment are designated S/T reference points. The connection between STU-R and STU-C may optionally contain one or more SHDSL signal regenerators (SRUs). The connections to the DLLs that interconnect STUs and SRUs are designated U reference points. For each STU-x and SRU, the Network side connection is termed the U-R interface and the Customer side connection is termed the U-C interface. The STU-C typically connects to a Central Office network at the V reference point.

5 Transport Capacity

This Recommendation specifies a two-wire operational mode for SHDSL transceivers that is capable of supporting user (payload) data rates from 192 kbit/s to 2.312 Mbit/s in increments of 8 kbit/s. The allowed rates are given by $n\times64 + i\times8$ kbit/s, where $3 \le n \le 36$ and $0 \le i \le 7$. For n=36, i is restricted to the values of 0 or 1. See Annex A and Annex B for details of specific regional requirements.

This Recommendation also specifies an optional four-wire operational mode that is capable of supporting user (payload) data rates from 384 kbit/s to 4.624 Mbit/s in increments of 16 kbit/s. Again, see Annex A and Annex B for details of specific regional requirements.

6 PMD Layer Functional Characteristics

6.1 Data Mode Operation

6.1.1 STU Data Mode PMD Reference Model

A reference model of the data mode PMD layer of an STU-C or STU-R transmitter is shown in Figure 6-1.

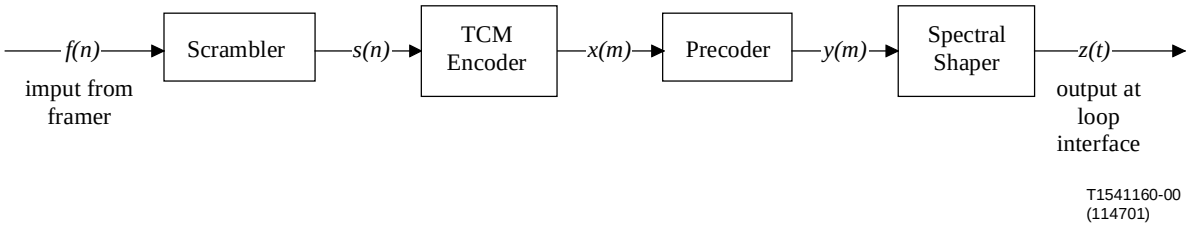


FIGURE 6-1

Data Mode PMD Reference Model

The time index *n* represents the bit time, the time index *m* represents the symbol time, and *t* represents analogue time. The input from the framer is *f(n)*, and *s(n)* is the output of the scrambler. Both the framer and the scrambler are contained within the PMS-TC layer and are shown here for clarity. *x(m)* is the output of the TCM (Trellis Coded Modulation) encoder, *y(m)* is the output of the channel precoder, and *z(t)* is the analogue output of the spectral shaper at the loop interface. When transferring *K* information bits per one-dimensional PAM symbol, the symbol duration is *K* times the bit duration, so the *K* values of *n* for a given value of *m* are {*mK*+0 , *mK*+1, …, *mK*+*K*-1}.

In the optional four-wire mode, two separate PMD sublayers are active - one for each wire pair. In this case, *n* represents the bit time for each wire pair rather than the aggregate system line rate.

6.1.1.1 PMD Rates

The operation of the PMD layer at the specified information rate shall be as specified in § A.5.1 or § B.5.1.

6.1.2 TCM Encoder

The block diagram of the TCM encoder is shown in Figure 6-2. The serial bit stream from the scrambler, *s(n)*, shall be converted to a *K*-bit parallel word at the *m*th symbol time, then processed by the convolutional encoder. The resulting *K*+1-bit word shall be mapped to one of 2^{K+1} pre-determined levels forming *x(m)*.

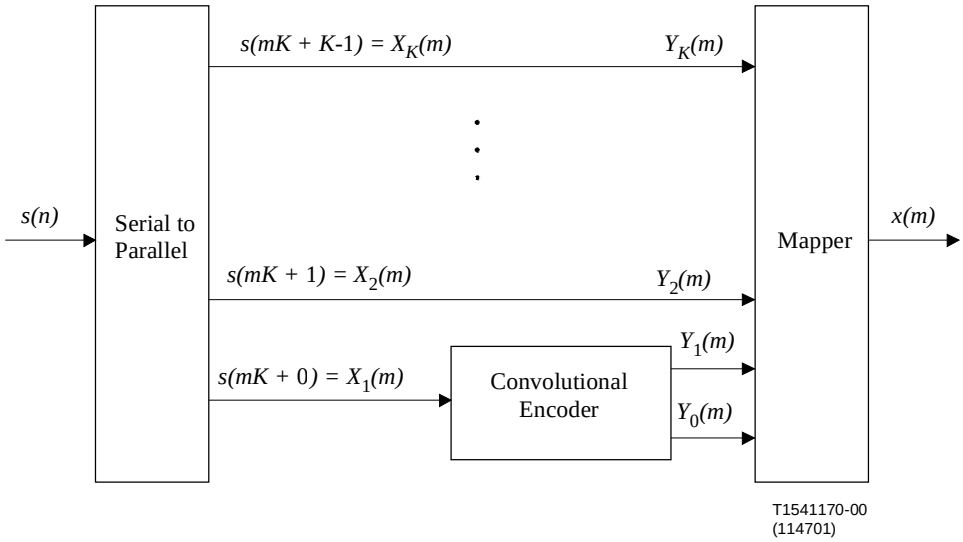


FIGURE 6-2

Block Diagram of the TCM Encoder

6.1.2.1 Serial-to-parallel converter

The serial bit stream from the scrambler, *s(n)*, shall be converted to a *K*-bit parallel word $\{X_1(m)=s(mK+0), X_2(m)=s(mK+1), \ldots, X_K(m)=s(mK+K-1)\}$ at the *m*th symbol time, where $X_1(m)$ is the first input bit in time.

6.1.2.2 Convolutional encoder

Figure 6-3 shows the feedforward non-systematic convolutional encoder, where T_s is a delay of one symbol time, "⊕" is binary exclusive-OR, and "⊗" is binary AND. $X_1(m)$ shall be applied to the convolutional encoder, $Y_1(m)$ and $Y_0(m)$ shall be computed, then $X_1(m)$ shall be shifted into the shift register.

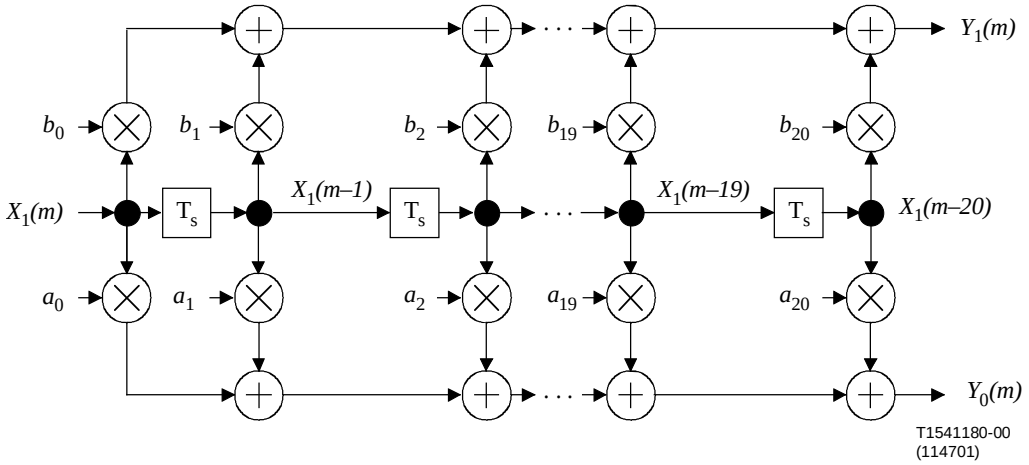


FIGURE 6-3

Block Diagram of the Convolutional Encoder

The binary coefficients a_i and b_i shall be passed to the encoder from the receiver during the activation phase specified in § 7.2.1.3. A numerical representation of these coefficients is *A* and *B* where:

$$A = a_{20}\bullet 2^{20}+a_{19}\bullet 2^{19}+a_{18}\bullet 2^{18}+...+a_0\bullet 2^0, \text{ and } B = b_{20}\bullet 2^{20}+b_{19}\bullet 2^{19}+b_{18}\bullet 2^{18}+...+b_0\bullet 2^0$$

The choice of encoder coefficients is vendor specific. They shall be chosen such that the system performance requirements are satisfied (see Annex A and/or Annex B for performance requirements).

6.1.2.3 Mapper

The K+1 bits $Y_K(m)$, …, $Y_1(m)$, and $Y_0(m)$ shall be mapped to a level $x(m)$. Table 6-1 gives the bit to level mapping for 16 level mapping.

TABLE 6-1

Mapping of bits to PAM levels

Y_3(m)	Y_2(m)	Y_1(m)	Y_0(m)	x(m) for 16-PAM
0	0	0	0	–15/16
0	0	0	1	–13/16
0	0	1	0	–11/16
0	0	1	1	–9/16
0	1	0	0	–7/16
0	1	0	1	–5/16
0	1	1	0	–3/16
0	1	1	1	–1/16
1	1	0	0	1/16
1	1	0	1	3/16
1	1	1	0	5/16
1	1	1	1	7/16
1	0	0	0	9/16
1	0	0	1	11/16
1	0	1	0	13/16
1	0	1	1	15/16

6.1.3 Channel Precoder

The block diagram of channel precoder is shown in Figure 6-4, where T_s is a delay of one symbol time.

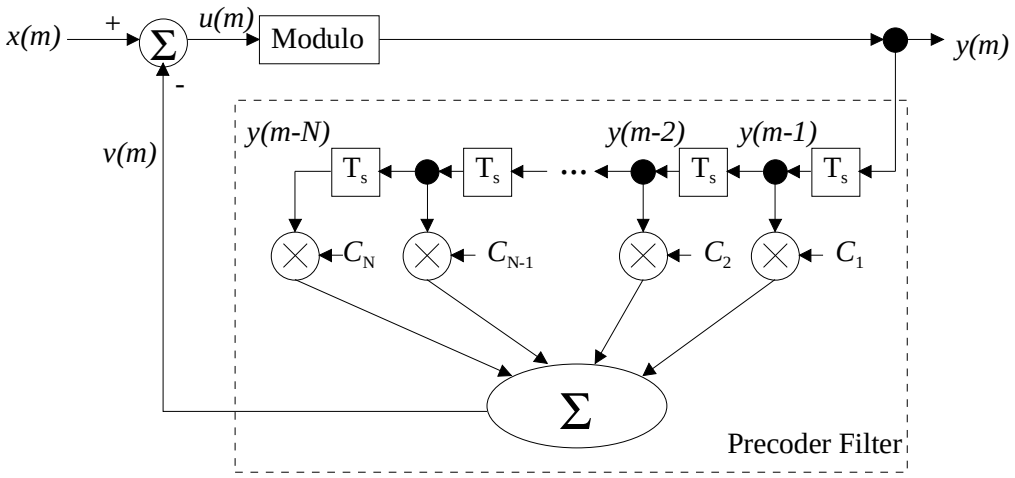


FIGURE 6-4

Block Diagram of the Channel Precoder

The coefficients of the precoder filter, C_k, shall be transferred to the channel precoder as described in § 7.2.1.2. The output of the precoder filter, *v(m)*, shall be computed as follows:

$$v(m) = \sum_{k=1}^{N} C_k \, y(m-k)$$

Where $128 \leq N \leq 180$. The function of the modulo block shall be to determine y(m) as follows: for each value of *u(m)*, find an integer, *d(m)*, such that:

$$-1 \leq u(m) + 2d(m) < 1$$

and then

$$y(m) = u(m) + 2d(m)$$

6.1.4 Spectral Shaper

The choice of spectral shape shall be region-specific. The details of PSDs for Regions A and B are given in § A.3.3.8 and § B.4.

6.1.5 Power Backoff

SHDSL devices shall implement Power Backoff, as specified in this section. The selected power backoff value shall be communicated during preactivation through the use of G.994.1 parameter selections.

The power backoff value shall be selected to meet the requirements shown in Table 6-2. The power backoff calculations are based on Estimated Power Loss (EPL), which is defined as:

Estimated Power Loss (dB) = TX Power (dBm) – Estimated RX Power (dBm), evaluated for the data mode PSD.

No explicit specification is given herein for the method of calculating Estimated RX Power. Depending upon the application, this value may be determined based on line probe results, *a priori* knowledge, or G.994.1 tone levels.

The Power Backoff that is applied shall be no less than the Default Power Backoff, and it shall not exceed the Maximum Power Backoff Value.

TABLE 6-2

Required Power Backoff Values

Estimated Power Loss (dB)	Maximum Power Backoff (dB)	Default Power Backoff (dB)
EPL > 6	31	0
6 ≥ EPL > 5	31	1
5 ≥ EPL > 4	31	2
4 ≥ EPL > 3	31	3
3 ≥ EPL > 2	31	4
2 ≥ EPL > 1	31	5
1 ≥ EPL > 0	31	6

6.2 PMD Activation Sequence

This section describes waveforms at the loop interface and associated procedures during Activation mode. The direct specification of the performance of individual receiver elements is avoided when possible. Instead, the transmitter characteristics are specified on an individual basis and the receiver performance is specified on a general basis as the aggregate performance of all receiver elements. Exceptions are made for cases where the performance of an individual receiver element is crucial to interoperability. In § 6.2.2, "convergence" refers to the state where all adaptive elements have reached steady-state. The declaration of convergence by a transceiver is therefore vendor dependent. Nevertheless, actions based on the state of convergence are specified to improve interoperability.

6.2.1 PMD Activation Reference Model

The reference model of the Activation mode of an STU-C or STU-R transmitter is shown in Figure 6-5.

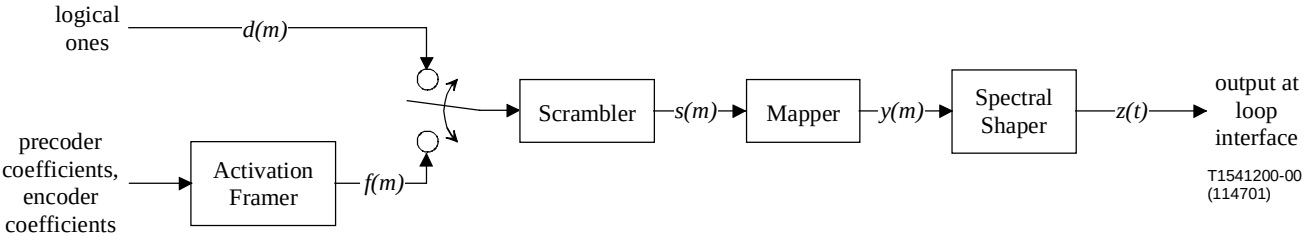


FIGURE 6-5

Activation Reference Model

The time index *m* represents the symbol time, and *t* represents analogue time. Startup uses 2-PAM modulation, so the bit time is equivalent to the symbol time. The output of the activation framer is *f(m)*, the framed information bits. The output of the scrambler is *s(m)*. Both the framer and the scrambler are contained within the PMS-TC layer and are shown here only for clarity. The output of the mapper is *y(m)*, and the output of the spectral shaper at the loop interface is *z(t)*. *d(m)* is an initialization signal that shall be logical ones for all *m*. The modulation format shall be uncoded 2-PAM, at the symbol rate selected for data mode operation.

In devices supporting the optional four-wire mode, the activation procedure shall be considered as an independent procedure for each pair. Such devices shall be capable of detecting the completion of activation for both pairs and upon completion shall initiate the transmission of user data over both pairs.

6.2.2 PMD Activation Sequence Description

The timing diagram for the activation sequence is given in Figure 6-6. The state transition diagram for the startup sequence is given in Figure 6-7. Each signal in the activation sequence shall satisfy the tolerance values listed in Table 6-3.

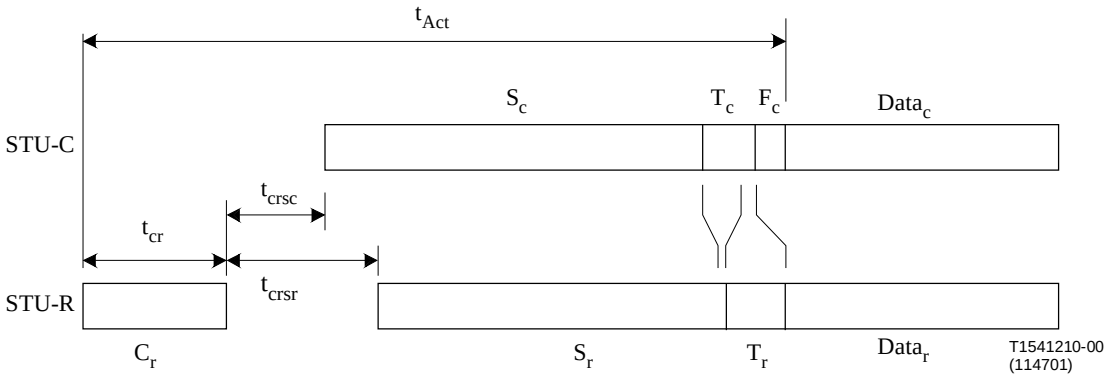


FIGURE 6-6

Timing Diagram for Activation Sequence

Figure 6-6A shows the total activation sequence at a high level for G.991.2, which includes pre-activation and core activation. Included as an example in the pre-activation phase are two sessions of handshake per G.994.1 and line probe.

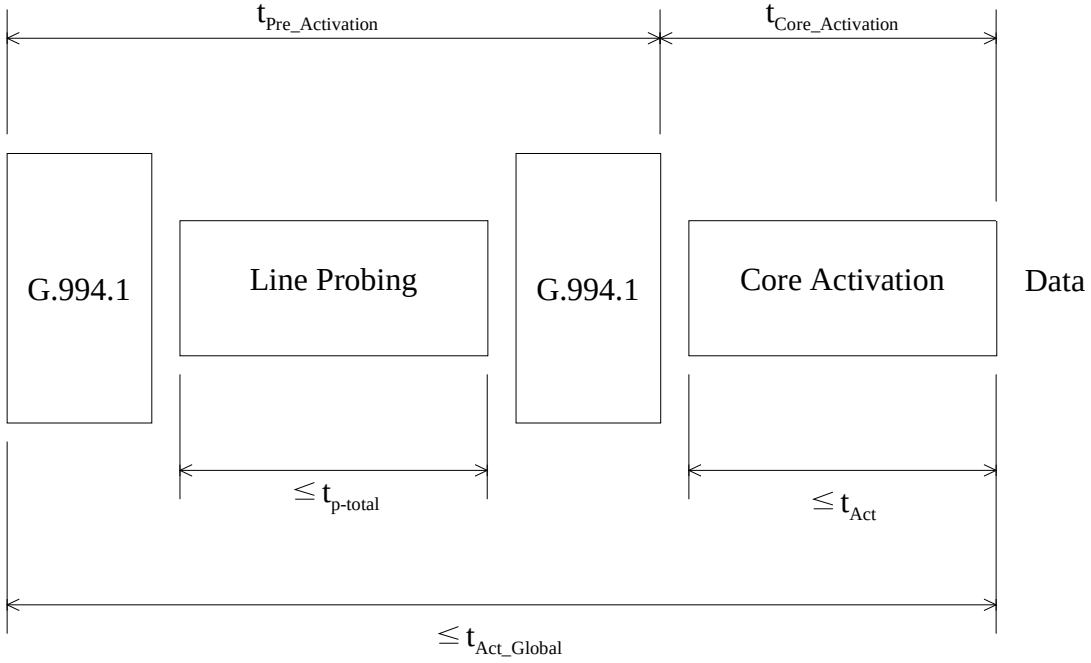


FIGURE 6-6A

G.991.2 Total Activation Sequence.

The global activation time is the sum of the pre-activation and core activation times. Therefore, from Figure 6-6A,

$$t_{Pre-activation} + t_{Core-Activationl} \leq t_{Act\_Global}$$

where $t_{Pre\text{-}activation}$ is the combined duration of the G.994.1 sessions (see § 6.4) and line probing (see § 6.3), $t_{Core\text{-}activation}$ is the core activation duration (see § 6.2). The values for t_{Act} and t_{Act_Global} are defined in Table 6-3. The value for $t_{p\text{-}total}$ is given in Table 6-5.

TABLE 6-3

Timing for Activation Signals

Time	Parameter	Reference	Nominal Value	Tolerance
t_{cr}	Duration of C_r	§ 6.2.2.1	1×β s *	±20 ms
t_{crsc}	Time from end of C_r to beginning of S_c	§ 6.2.2.2	500 ms	±20 ms
t_{crsr}	Time from end of C_r to beginning of S_r	§ 6.2.2.3	1.5×β s *	±20 ms
t_{Act}	Maximum time from start of C_r to $Data_r$		15×β s *	
$t_{PayloadValid}$	Maximum time from start of $Data_c$ or $Data_r$ to valid SHDSL payload data		1 s	
$t_{Silence}$	Minimum silence time from exception condition to start of train		2 s	
t_{PLL}	Maximum time from start of S_c to STU-R PLL lock		5 s	
t_{Act_Global}	Maximum time from start of initial pre-activation session (§ 6.3) to $Data_r$		30 s	
* β is dependent on bit rate. β=1 for n>12, β=2 for n≤12, where n is defined in § 5.				

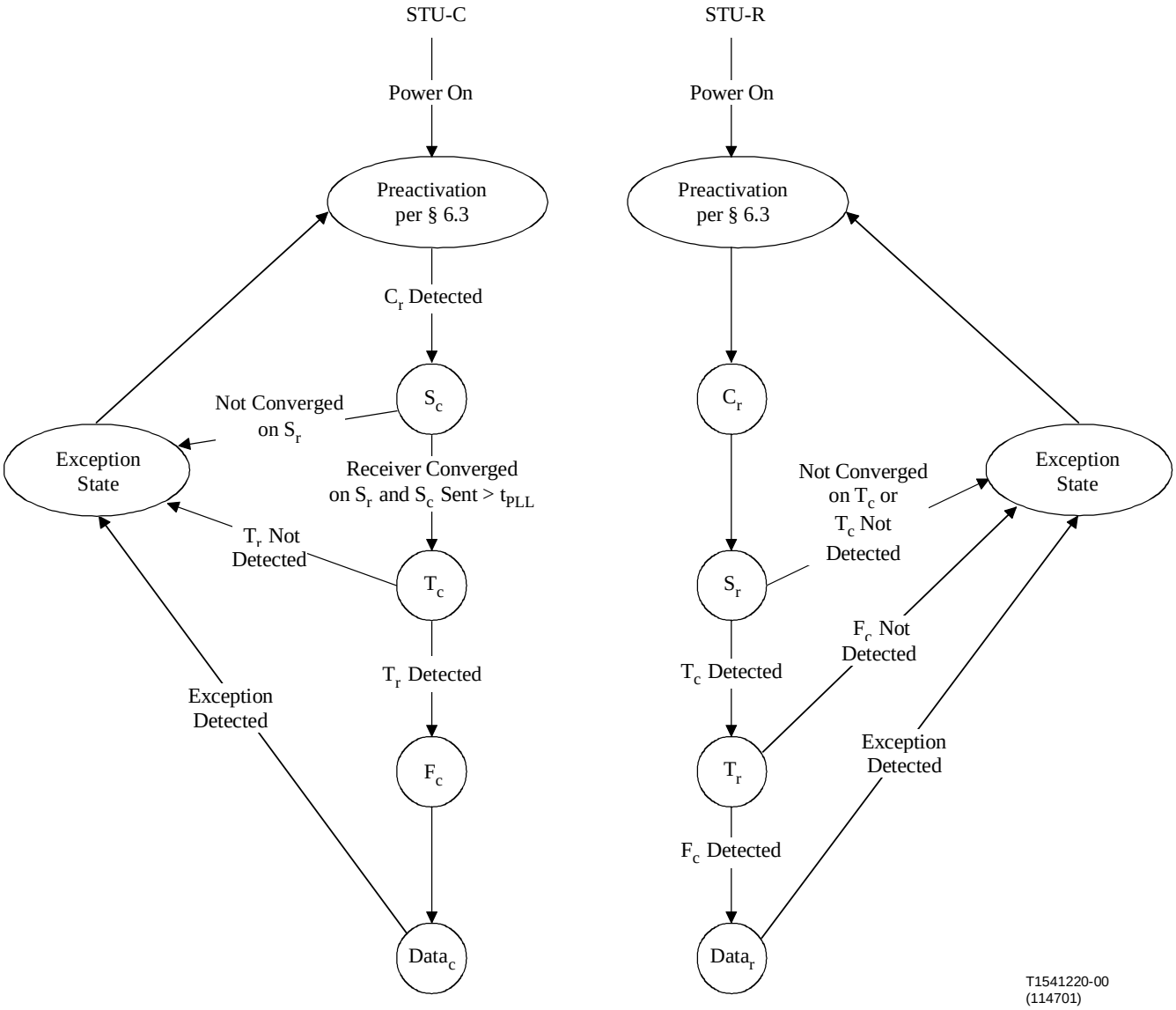


FIGURE 6-7

STU-C and STU-R Transmitter Activation State Transition Diagram

6.2.2.1 Signal C_r

After exiting the preactivation sequence (per G.994.1 [2], see § 6.3 for details), the STU-R shall send C_r. Waveform C_r shall be generated by connecting the signal *d(m)* to the input of the STU-R scrambler as shown in Figure 6-5. The PSD mask for C_r shall be the upstream PSD mask, as negotiated during preactivation sequence. C_r shall have a duration of t_{cr} and shall be sent 0.3 s after the end of preactivation.

6.2.2.2 Signal S_c

After detecting C_r, the STU-C shall send S_c. Waveform S_c shall be generated by connecting the signal *d(m)* to the input of the STU-C scrambler as shown in Figure 6-5. The PSD mask for S_c shall be the downstream PSD mask, as negotiated during preactivation sequence. S_c shall be sent t_{crsc}

after the end of C_r. If the STU-C does not converge while S_c is transmitted, it shall enter the exception state (§ 6.2.2.8).

6.2.2.3 Signal S_r

The STU-R shall send S_r, beginning t_{crsr} after the end of C_r. Waveform S_r shall be generated by connecting the signal *d(m)* to the input of the STU-R scrambler as shown in Figure 6-5. The PSD mask for S_r shall be the same as for C_r. If the STU-R does not converge and detect T_c while S_r is transmitted, it shall enter the exception state (§ 6.2.2.8). The method used to detect T_c is vendor dependent. In timing modes supporting loop timing, waveform S_r and all subsequent signals transmitted from the STU-R shall be loop timed, i.e., the STU-R symbol clock shall be locked to the STU-C symbol clock.

6.2.2.4 Signal T_c

Once the STU-C has converged and has been sending S_c for at least t_{PLL} (Table 6-3), it shall send T_c. Waveform T_c contains the precoder coefficients and other system information. T_c shall be generated by connecting the signal *f(m)* to the input of the STU-C scrambler as shown in Figure 6-5. The PSD mask for T_c shall be the same as for S_c. The signal *f(m)* is the activation frame information as described in § 7.2.1. If the STU-C does not detect T_r while sending T_c, it shall enter the exception state (§ 6.2.2.8). The method used to detect T_r is vendor dependent.

6.2.2.5 Signal T_r

Once the STU-R has converged and has detected the T_c signal, it shall send T_r. Waveform T_r contains the precoder coefficients and other system information. T_r shall be generated by connecting the signal *f(m)* to the input of the STU-R scrambler as shown in Figure 6-5. The PSD mask for T_r shall be the same as for C_r. The signal *f(m)* is the activation frame information as described in § 7.2.1. If the STU-R does not detect F_c while sending T_r, it shall enter the exception state (§ 6.2.2.8). The method used to detect F_c is vendor dependent.

6.2.2.6 Signal F_c

Once the STU-C has detected T_r and completed sending the current T_c frame, then it shall send F_c. The first bit of the first F_c frame shall follow contiguously the last bit of the last T_c frame. Signal F_c shall be generated by connecting the signal *f(m)* to the input of the STU-C scrambler as shown in Figure 6-5. The PSD mask for F_c shall be the same as for S_c. The signal *f(m)* is the activation frame information as described in § 7.2.1 with the following exceptions: the frame sync word shall be reversed in time, and the payload information bits shall be set to arbitrary values. The CRC shall be calculated on this arbitrary-valued payload. The signal F_c shall be transmitted for exactly two activation frames. As soon as the first bit of F_c is transmitted, the payload data in the T_r signal shall be ignored.

6.2.2.7 $Data_c$ and $Data_r$

Within 200 symbols after the end of the second frame of F_c, the STU-C shall enter data mode and send $Data_c$, and the STU-R shall enter data mode and send $Data_r$. These TCPAM signals are described in § 6.1. The PSD mask for $Data_r$ and for $Data_c$ shall be according to § A.4 or § B.4, as negotiated during the preactivation sequence. There is no required relationship between the end of the activation frame and any bit within the SHDSL data-mode frame. $t_{PayloadValid}$ (Table 6-3) after the end of F_c, the SHDSL payload data shall be valid at the α or β interface.

6.2.2.8 Exception State

If activation is not achieved within t_{act} (Table 6-3) or if preactivation and activation are not completed within t_{act_global} (Table 6-3) or if any exception condition occurs, then the exception state shall be invoked. During the exception state the STU shall be silent for at least $t_{silence}$ (Table 6-3), then wait for transmission from the far end to cease, then return to the corresponding initial startup state; the STU-R and STU-C shall begin preactivation, as per § 6.3.

6.2.2.9 Exception Condition

An exception condition shall be declared during activation if any of the timeouts in Table 6-3 expire or if any vendor-defined abnormal event occurs. An exception condition shall be declared during data mode if a vendor-defined abnormal event occurs. A vendor-defined abnormal event shall be defined as any event that requires a loop restart for recovery.

6.2.3 Framer and Scrambler

The activation mode framer and scrambler are described in § 7.2.

6.2.4 Mapper

The output bits from the scrambler, *s(m)*, shall be mapped to the output level, *y(m)*, as follows:

TABLE 6-4

Bit-to-Level Mapping

Scrambler Output *s(m)*	Mapper Output Level, *y(m)*	Data Mode Index
0	–9/16	0011
1	+9/16	1000

These levels, corresponding to the scrambler outputs 0 and 1, shall be identical to the levels in the 16-TCPAM constellation (Table 6-1) corresponding to indexes 0011 and 1000, respectively.

6.2.5 Spectral Shaper

The same spectral shaper shall be used for data mode and activation mode as described in § A.4 or § B.4.

6.2.6 Timeouts

Table 6-3 shows the system timeouts and their values. t_{act} shall be the maximum time from the start of C_r to the start of $Data_r$. It controls the overall time of the train. $t_{PayloadValid}$ is the time between the start of data mode and the instant at which the SHDSL payload data is valid (this accounts for settling time, data flushing, frame synchronization, etc). $t_{Silence}$ shall be the minimum time in the exception state in which the STU-C or STU-R is silent before returning to preactivation (per G.994.1 [2], see § 6.3 for details). t_{PLL} shall be the time allocated for the STU-R to pull in the STU-C timing. The STU-C shall transmit S_c for at least t_{PLL}.

6.3 PMD Preactivation Sequence

This section describes waveforms at the loop interface and associated procedures during preactivation mode. The direct specification of the performance of individual receiver elements is

avoided when possible. Instead, the transmitter characteristics are specified on an individual basis and the receiver performance is specified on a general basis as the aggregate performance of all receiver elements. Exceptions are made for cases where the performance of an individual receiver element is crucial to interoperability.

In the optional four-wire mode, Pair 1 and Pair 2 shall be determined during the preactivation sequence. Pair 1 shall be defined as the pair on which the final G.994.1 transaction is conducted.

6.3.1 PMD Preactivation Reference Model

The reference model of the Preactivation mode of an STU-C or STU-R transmitter is shown in Figure 6-8.

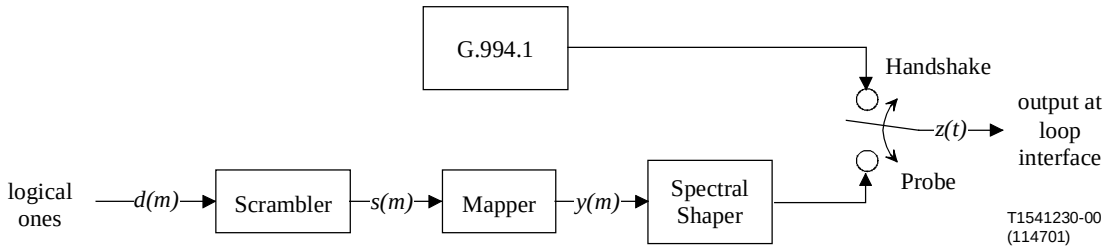


FIGURE 6-8

Preactivation Reference Model

The time index *m* represents the symbol time, and *t* represents analogue time. Since the probe signal uses 2-PAM modulation, the bit time is equivalent to the symbol time. The output of the scrambler is *s(m)*. The scrambler used in the PMD preactivation may differ from the PMS-TC scrambler used in activation and data modes. See § 6.3.3 for details of the preactivation scrambler. The output of the mapper is *y(m)*, and the output of the spectral shaper at the loop interface is *z(t)*. *d(m)* is an initialization signal that shall be logical ones for all *m*. The probe modulation format shall be uncoded 2-PAM, with the symbol rate, spectral shape, duration and power backoff selected by G.994.1. Probe results shall be exchanged by G.994.1.

In the optional four-wire mode, the G.994.1 exchange shall follow the defined procedures for multi-pair operation. In this case, Signals P_{ri} and P_{ci}, as described below, shall be sent in parallel on both wire pairs.

6.3.2 PMD Preactivation Sequence Description

A typical timing diagram for the preactivation sequence is given in Figure 6-9. Each signal in the preactivation sequence shall satisfy the tolerance values listed in Table 6-5.

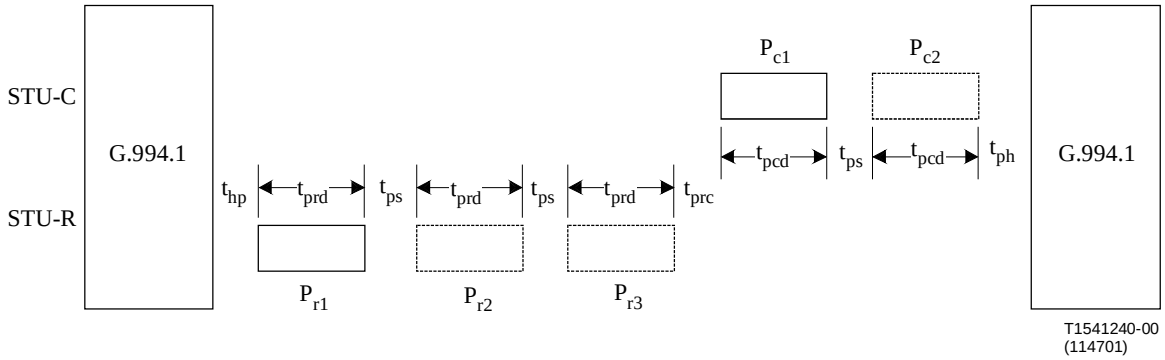


FIGURE 6-9

Typical Timing Diagram for Preactivation Sequence

TABLE 6-5

Timing for Preactivation Signals[1]

Time	Parameter	Nominal Value	Tolerance
t_{hp}	Time from end of handshake to start of remote probe	0.2 s	±10 ms
t_{prd}	Duration of remote probe	Selectable from 50 ms to 3.1 s	±10 ms
t_{ps}	Time separating two probe sequences	0.2 s	±10 ms
t_{prc}	Time separating last remote and first central probe sequences	0.2 s	±10 ms
t_{pcd}	Duration of central probe	Selectable from 50 ms to 3.1 s	±10 ms
t_{ph}	Time from end of central probe to start of handshake	0.2 s	±10 ms
$t_{p\text{-}total}$	Total probe duration, from end of the first G.994.1 session to the start of the second G.994.1 session	10 s maximum	

6.3.2.1 Signal P_{ri}

If the optional line probe is selected during the G.994.1 session (see G.994.1 [2] for details), the STU-R shall send the remote probe signal. The symbol rate for the remote probe signal shall be negotiated during the G.994.1 session, and shall correspond to the symbol rate used during activation for the specified data rate. If multiple remote probe symbol rates are negotiated during

[1] Tolerances are relative to the nominal or ideal value. They are not cumulative across the preactivation sequence.

the G.994.1 session, then multiple probe signals will be generated, starting with the lowest symbol rate negotiated and ending with the highest symbol rate negotiated. P_{ri} is the ith probe signal (corresponding to the ith symbol rate negotiated). Waveform P_{ri} shall be generated by connecting the signal *d(m)* to the input of the STU-R scrambler as shown in The PSD mask for P_{ri} shall be the upstream PSD mask used for signal C_r at the same symbol rate, and shall be selectable between the PSDs for activating at data rates of 192 kbit/s to 2 304 kbit/s in steps of 64 kbit/s. Alternatively, waveform P_{ri} can be selected to transmit silence. The duration (t_{prd}) and power backoff shall be the same for all P_{ri}, and shall be negotiated during the G.994.1 session. The duration shall be selectable between 50 ms and 3.1 s in steps of 50 ms, and the power backoff shall be selectable between 0 dB and 15 dB in steps of 1 dB. The probe signal power backoff can be selected using either the received G.994.1 signal power or *a priori* knowledge. If no information is available, implementors are encouraged to select a probe power backoff of at least 6 dB. The first remote probe signal shall begin t_{hp} after the end of the G.994.1 session. There shall be a t_{ps} second silent interval between successive remote probe signals.

In the optional four-wire mode, P_{ri} shall be sent in parallel on both wire pairs.

6.3.2.2 Signal P_{ci}

The STU-C shall send the central probe signal t_{prc} after the end of the last remote probe signal. The symbol rate for the central probe signal shall be negotiated during the G.994.1 session, and shall correspond to the symbol rate used during activation for the specified data rate. If multiple central probe symbol rates are negotiated during the G.994.1 session, then multiple probe signals will be generated, starting with the lowest symbol rate negotiated and ending with the highest symbol rate negotiated. Waveform P_{ci} is the ith probe signal (corresponding to the ith symbol rate negotiated). Waveform P_{ci} shall be generated by connecting the signal *d(m)* to the input of the STU-C scrambler as shown in The PSD mask for P_{ci} shall be the downstream PSD mask used for signal S_c at the same symbol rate, and shall be selectable between the PSDs for activating at data rates of 192 kbit/s to 2 304 kbit/s in steps of 64 kbit/s. Alternatively, waveform P_{ri} can be selected to transmit silence. The duration (t_{pcd}) and power backoff shall be the same for all P_{ci}, and shall be negotiated during the G.994.1 session. The duration shall be selectable between 50 ms and 3.1 s in steps of 50 ms, and the power backoff shall be selectable between 0 dB and 15 dB in steps of 1 dB. The probe signal power backoff can be selected using either the received G.994.1 signal power or a priori knowledge. If no information is available, implementors are encouraged to select a probe power backoff of at least 6 dB. There shall be a t_{ps} silent interval between successive central probe signals, and there shall be a t_{ph} second silent interval between the last central probe signal and the start of the following G.994.1 session.

In the optional four-wire mode, P_{ci} shall be sent in parallel on both wire pairs.

6.3.3 Scrambler

The preactivation mode scrambler shall have the same basic structure as the data mode scrambler, but may employ a different scrambler polynomial. During the G.994.1 session, the scrambler polynomial for the line probe sequence shall be selected by the receiver from the set of allowed scrambler polynomials listed in Table 6-6. The transmitter shall support all the polynomials in Table 6-6. During the line probe sequence, the transmit scrambler shall use the scrambler polynomial selected by the receiver during the G.994.1 session. The scrambler shall be initialized to all zeros.

TABLE 6-6

Preactivation Scrambler Polynomials

Polynomial Index (i_2,i_1,i_0)	STU-C polynomial	STU-R polynomial
0 0 0	$s(m) = s(m-5) \oplus s(m-23) \oplus d(m)$	$s(m) = s(m-18) \oplus s(m-23) \oplus d(m)$
0 0 1	$s(m) = s(m-1) \oplus d(m)$	$s(m) = s(m-1) \oplus d(m)$
0 1 0	$s(m) = s(m-2) \oplus s(m-5) \oplus d(m)$	$s(m) = s(m-3) \oplus s(m-5) \oplus d(m)$
0 1 1	$s(m) = s(m-1) \oplus s(m-6) \oplus d(m)$	$s(m) = s(m-5) \oplus s(m-6) \oplus d(m)$
1 0 0	$s(m) = s(m-3) \oplus s(m-7) \oplus d(m)$	$s(m) = s(m-4) \oplus s(m-7) \oplus d(m)$
1 0 1	$s(m) = s(m-2) \oplus s(m-3) \oplus s(m-4) \oplus s(m-8) \oplus d(m)$	$s(m) = s(m-4) \oplus s(m-5) \oplus s(m-6) \oplus s(m-8) \oplus d(m)$
1 1 0	Reserved	Reserved
1 1 1	Not Allowed	Not Allowed

6.3.4 Mapper

The output bits from the scrambler, *s(m)*, shall be mapped to the output level, *y(m)*, as described in § 6.2.4.

6.3.5 Spectral Shaper

The same spectral shaper shall be used for data mode and activation mode as described in § 6.1.4.

6.3.6 PMMS Target Margin

PMMS target margin is used by the receiver to determine if a data rate can be supported with this margin under current noise and/or reference worst-case noise specified in Annex A and Annex B. A data rate may be included in the capabilities list resulting from line probe only if the estimated SNR associated with that data rate minus the SNR required for BER=10^{-7} is greater than or equal to target margin in dB. If both worst-case target margin and current-condition target margin are specified, then the capabilities exchanged shall be the intersection of data rates calculated using each noise condition separately.

The use of negative target margins with respect to reference worst-case noise corresponds to reference noise with fewer disturbers. This may be applicable when the number of disturbers is known to be substantially fewer than specified by the reference worst-case noise. Use of negative target margins with respect to current-conditions is not advised. Use of the current-condition target margin mode may result in retrains if the noise environment changes significantly.

6.4 G.994.1 Preactivation Sequence

As noted in § 6.3, G.994.1 [2] shall be used to begin the preactivation sequence. A second G.994.1 sequence shall follow the preactivation line probe, as described in that section. The G.994.1 protocol shall be the mechanism for exchanging capabilities and negotiating the operational parameters for each SHDSL connection. The use of a line probe sequence, as described in § 6.3, is optional. If each STU has sufficient *a priori* knowledge of the line characteristics and the capabilities of the other STU, either from a previous connection or from user programming, the line

probe sequence may be bypassed. In this case, the G.994.1 sequence will be followed by SHDSL activation, as described in § 6.2.

6.4.1 G.994.1 Code Point Definitions

The following definitions shall be applied to the SHDSL parameters specified in G.994.1:

Training mode	An indication that an STU (or SRU) is prepared to begin SHDSL Activation using the associated parameters.
PMMS mode	An indication that an STU (or SRU) is prepared to begin a PMMS ("Power Measurement Modulation Session", or Line Probe) using the associated parameters.
Four-wire	Set to indicate four-wire operation.
SRU	Set to indicate that the unit is a Signal Regenerator and not an STU.
Diagnostic Mode	Set to indicate a diagnostic mode train (for use with SRUs).
Base Data Rate / PSD	These octets are used as follows: for PMMS, they indicate rates for line probing segments for training, they indicate payload data rates Separate bits are provided for symmetric and asymmetric PSDs.
Sub Data Rate	For symmetric PSDs, the Data Rate octets indicate the base data rate in 64 kbit/s increments ($n \times 64$ kbit/s). The Sub Data Rate bits indicate additional 8 kbit/s increments ($i \times 8$ kbit/s) of Data. The total payload data rate is set by: Base Data Rate + Sub Data Rate. The Sub Data Rate bits do not apply to the asymmetric 2.048 Mbit/s, and 2.304 Mbit/s PSDs (from Annex B). For the asymmetric 768 or 776 kbit/s and asymmetric 1.536 or 1.544 Mbit/s PSDs (from Annex A), the Base Data Rate bits indicate 768 kbit/s or 1.536 Mbit/s, and the Sub Data Rate bits for 0 and 8 kbit/s are valid for selecting the total payload data rate.
PBO	Power Backoff (in 1.0 dB increments).
PMMS Duration	The length of each line probe (PMMS) segment (in 50 ms increments).
PMMS Scrambler	The scrambler polynomial used during line probe (PMMS). See § 6.3.3.
PMMS Target Margin	If worst-case target margin is selected, target margin is relative to reference worst-case crosstalk specified in Table A-13 and Table B-14. If current-condition target margin is selected, specified target margin is relative to noise measured during line probe. The 5 bit target margin is specified by (bits 5-1 x 1.0 dB) - 10 dB. For example, 101111_2 in the worst-case PMMS target margin octet corresponds to 15 dB - 10dB = 5dB target margin relative to reference worst-case noise. If the capability for PMMS mode is indicated in a G.994.1 CLR/CL capabilities exchange, both target margin octets shall be sent. The specific values for target margin shall be ignored

	during the capabilities exchange, as all STUs (and SRUs) shall be capable of evaluating the results of PMMS using both types of target margin.
Clock Modes	Set to indicate clock mode, as defined in Table 10-1.
Low Latency	Set to indicate that low latency operation, as defined in § 11.5 is required. If not set, an STU may choose a higher latency encoding scheme.
TPS-TC	The TPS-TC mode is selected from the set of modes specified in Annex E.
Sync Word	Indicates the value that the upstream and downstream *sw1* - *sw14* bits shall take on. See § 7.1.2.1 for details.
Stuff Bits	Indicates the value that the upstream and downstream *stb1* - *stb4* bits shall take on. See § 7.1.2.7 for details.
Regenerator Silent Period (RSP)	A bit used to force an STU or SRU into a 1-minute silent interval to facilitate startup of spans including regenerators.

6.4.2 G.994.1 Tone Support

SHDSL devices shall support half-duplex mode G.994.1 operation using the A4 carrier set from the 4 kHz signalling family. Manufacturers are encouraged to support additional carrier sets, the 4.3125 kHz signalling family, and full-duplex operation of G.994.1 to provide interoperable handshake sequences with other types of DSL equipment.

6.4.3 G.994.1 Transactions

If no *a priori* capabilities information is available to the STU-R, it should begin the G.994.1 session by initiating Transaction C (CLR/CL). Otherwise, it may begin immediately with one of the mode selection transactions (e.g. A or B). In this capabilities exchange (CLR/CL sequence), each unit shall indicate the functions that it is currently capable of performing. This means that user options that have been disabled shall not be indicated as capabilities of the unit. If a unit's capabilities change due to user option settings or other causes, that unit shall cause a capabilities exchange to occur during the next G.994.1 session.

If both the STU-R and STU-C indicate the capability for line probing and no *a priori* information exists concerning the characteristics of the loop, the STU-R should initiate Transaction D (MP/MS/Ack(1)) by sending an MP with the G.991.2 line probe mode selected. This MP message shall include parameters for the downstream line probe sequence. The STU-C shall then issue a corresponding MS message containing the upstream line probe parameters and an echo of the downstream line probe parameters. Following an Ack(1) from the STU-R, the units shall exit G.994.1 and enter the G.991.2 line probe mode, as described in § 6.3. Following the completion of line probing, the STU-C shall initiate a new G.994.1 session. The STU-R shall then initiate a Transaction C (CLR/CL) capabilities exchange to indicate the results of the line probe. Each unit shall, in this exchange, indicate the intersection of its capabilities and the capabilities of the loop, as determined during the line probe sequence. The PBO octet shall be used to indicate the desired received Power Backoff. Following this second capabilities exchange, the units may use any valid transaction to select operational SHDSL parameters.

Following the selection of the G.991.2 parameter set, G.994.1 shall terminate and the SHDSL Activation sequence (§ 6.2) shall begin.

6.4.4 Operation with Signal Regenerators

In general, SRUs will act as STUs during G.994.1, as described in § 6.4.3. In some situations, however, they are required to issue "Regenerator Silent Period" (via the G.994.1 RSP bit) mode selections rather than selecting a G.991.2 operational mode, as described in Annex D and Appendix II. The parameters that SRUs report during capabilities exchanges are also slightly different. The advertised capabilities of an SRU-R shall be the intersection of its own capabilities and those reported across the regenerator's internal interface as indicative of the capabilities of the downstream units and line segments. The lone exception to this rule shall be the PBO octet, which shall be considered as a local parameter for each segment.

7 PMS-TC Layer Functional Characteristics

7.1 Data Mode Operation

7.1.1 Frame Structure

Table 7-1 summarizes the SHDSL frame structure. Complete bit definitions may be found in § 7.1.2.

The size of each payload block is defined as k bits, where $k = 12\ (i + n \times 8)$ [bits]. The payload data rate is set by: $n \times 64 + i \times 8$ kbit/s, where $3 \leq n \leq 36$ and $0 \leq i \leq 7$. For n=36, i is restricted to the values of 0 or 1. The value of i shall be negotiated during startup, and shall apply to all values of n. The selected value of i applies to all values of n, will be negotiated during preactivation, and does not include the 8 kbit/s framing overhead.

In the optional four-wire mode, two separate PMS-TC sublayers are active - one for each wire pair. In this case, the above formula represents the payload data rate for each pair rather than the aggregate payload rate. Each pair shall operate at the same payload rate, and the transmitters for both pairs shall maintain frame alignment within specified limits. In the STU-C, the symbol clocks for each pair shall be derived from a common source. The maximum differential delay between the start of STU-C frames shall be no greater than four (4) symbols at the line side of each SHDSL transmitter. In the STU-R, symbol clocks may be derived from loop timing on each pair, so these clocks shall be locked in frequency but shall have an arbitrary phase relationship. The maximum differential delay between the start of STU-R frames shall be no greater than six (6) symbols at the line side of each SHDSL transmitter.

TABLE 7-1

SHDSL Frame Structure

Time	Frame Bit #	Over-head Bit #	Name	Description	Notes
0 ms	1-14	1-14	*sw1-sw14*	Frame Sync Word	
	15	15	*fbit1/losd*	Fixed Indicator bit #1 (Loss of Signal)	
	16	16	*fbit2/sega*	Fixed Indicator bit #2 (Segment Anomaly)	
	17 -> *k*+16	---------	*b1*	Payload block #1	
	k + 17	17	*eoc01*	EOC bit #1	
	k + 18	18	*eoc02*	EOC bit #2	
	k + 19	19	*eoc03*	EOC bit #3	
	k + 20	20	*eoc04*	EOC bit #4	
	k + 21	21	*crc1*	Cyclic Redundancy Check #1	CRC-6
	k + 22	22	*crc2*	Cyclic Redundancy Check #2	CRC-6
	k + 23	23	*fbit3/ps*	Fixed Indicator bit #3 (Power Status)	
	k + 24	24	*sbid1*	Stuff bit ID #1	Spare in synchronous mode
	k + 25	25	*eoc05*	EOC bit #5	
	k + 26	26	*eoc06*	EOC bit #6	
	k + 27 -> 2*k* + 26	---------	*b2*	Payload block #2	
	2*k* + 27	27	*eoc07*	EOC bit #7	
	2*k* + 28	28	*eoc08*	EOC bit #8	
	2*k* + 29	29	*eoc09*	EOC bit #9	
	2*k* + 30	30	*eoc10*	EOC bit #10	
	2*k* + 31	31	*crc3*	Cyclic Redundancy Check #3	CRC-6
	2*k* + 32	32	*crc4*	Cyclic Redundancy Check #4	CRC-6
	2*k* + 33	33	*fbit4/segd*	Fixed Indicator bit #4 (Segment Defect)	
	2*k* + 34	34	*eoc11*	EOC bit #11	
	2*k* + 35	35	*eoc12*	EOC bit #12	
	2*k* + 36	36	*sbid2*	Stuff bit ID #2	Spare in synchronous mode
	2*k* + 37 -> 3*k* + 36	---------	*b3*	Payload block #3	
	3*k* + 37	37	*eoc13*	EOC bit #13	
	3*k* + 38	38	*eoc14*	EOC bit #14	
	3*k* + 39	39	*eoc15*	EOC bit #15	
	3*k* + 40	40	*eoc16*	EOC bit #16	
	3*k* + 41	41	*crc5*	Cyclic Redundancy Check #5	CRC-6

	3*k* + 42	42	*crc6*	Cyclic Redundancy Check #6	CRC-6
	3*k* + 43	43	*eoc17*	EOC bit #17	
	3*k* + 44	44	*eoc18*	EOC bit #18	
	3*k* + 45	45	*eoc19*	EOC bit #19	
	3*k* + 46	46	*eoc20*	EOC bit #20	
6 - 3/(*k*+12) ms	3*k* + 47 -> 4*k* + 46	---------	*b4*	Payload block #4	
	4*k* + 47	47	*stb1*	Stuff bit #1	Vendor dependent in synchronous mode
6 ms nominal	4*k* + 48	48	*stb2*	Stuff bit #2	Vendor dependent in synchronous mode
	4*k* + 49	49	*stb3*	Stuff bit #3	Not present in synchronous mode
6 + 3/(*k*+12) ms	4*k* + 50	50	*stb4*	Stuff bit #4	Not present in synchronous mode

7.1.2 Frame Bit Definitions

In Table 7-1, the bit sequence of the SHDSL frame (prior to scrambling at the transmit side and after descrambling at the receive side) is presented. The frame structures are identical in both upstream and downstream directions of transmission. Spare bits in either direction shall be set to 1.

The following frame bit definitions are used:

7.1.2.1 *sw1 - sw14* (Frame Sync Word)

The frame synchronization word (FSW) enables SHDSL receivers to acquire frame alignment. The FSW (bits *sw1 - sw14*) is present in every frame and is specified independently for the upstream and downstream directions.

7.1.2.2 *b1 - b4* (Payload Blocks)

Used to carry user data. The internal structure of the payload blocks is defined in § 8.1.

7.1.2.3 *eoc01 - eoc20* (Embedded Operations Channel)

20 bits (*eoc01...eoc20*) are provided as a separate maintenance channel. See § 9.5 for details. In four-wire mode, *eoc01 - eoc20* on Pair 1 shall be carry the primary EOC data. The corresponding Pair 2 *eoc* bits shall be duplicates of the Pair 1 *eoc* bits.

7.1.2.4 *crc1 - crc6* (Cyclic Redundancy Check code)

Six bits assigned to a cyclic redundancy check (CRC) code (see § 7.1.3).

7.1.2.5 *fbit1 - fbit4* (Fixed Indicator bits)

Used for the indication of time-critical framing information. Specific bit definitions are given below.

7.1.2.5.1 *fbit1 = losd* (Loss of Signal)

Used to indicate the loss of signal from the application interface. Loss of Signal = 0, Normal = 1. Definition of the conditions causing the indication of *losd* is vendor specific and beyond the scope

of this Recommendation. In four-wire mode, *losd* on Pair 1 shall carry the primary *losd* indication. The Pair 2 *losd* bit shall be a duplicate of the Pair 1 bit.

7.1.2.5.2 *fbit2 = sega* **(Segment Anomaly)**

Used to indicate a CRC error on the incoming SHDSL frame. A segment anomaly indicates that a regenerator operating on a segment has received corrupted data and therefore the regenerated data is unreliable. The purpose of segment anomaly is to ensure internal performance monitoring integrity; it is not intended to be reported to an external management entity. CRC Error = 0, Normal = 1.

7.1.2.5.2.1 STU Operation

The STU shall set the *sega* bit to 1.

7.1.2.5.2.2 SRU Operation

If a CRC error is declared for an incoming frame, an SRU shall set the *sega* bit to 0 in the next available outgoing frame in the forward direction, i.e. in the direction of the data over which the CRC error was observed. If no CRC error is declared then an SRU shall pass the *sega* bit without modification.

7.1.2.5.3 *fbit3 = ps* **(Power Status)**

The power status bit *ps* is used to indicate the status of the local power supply in the STU-R. The power status bit is set to 1 if power is normal and to 0 if the power has failed. On loss of power at the STU-R, there shall be enough power left to communicate three "Power Loss" messages towards the STU-C. Regenerators shall pass this bit transparently. In four-wire mode, *ps* on Pair 1 shall carry the primary power status indication. The Pair 2 *ps* bit shall be a duplicate of the Pair 1 *ps* bit.

7.1.2.5.4 *fbit4 = segd* **(Segment Defect)**

Used to indicate a loss of sync on the incoming SHDSL frame. A segment defect indicates that a regenerator has lost synchronization and therefore the regenerated data is unavailable. This bit is typically reported to an external management entity and is used to ensure timely protection switching, alarm filtering, etc. Loss of Sync = 0, Normal = 1.

7.1.2.5.4.1 STU Operation

The STU shall set the *segd* bit to 1.

7.1.2.5.4.2 SRU Operation

If a LOSW-Defect is declared, an SRU shall set the *segd* bit to 0 in the next available outgoing frame in the forward direction, i.e. in the direction of the data over which the LOSW-Defect was observed. If no LOSW-Defect is declared then an SRU shall pass the *segd* bit without modification.

7.1.2.6 *sbid1, sbid2* **(Stuff Indicator bits)**

In plesiochronous mode, the stuff indicator bits indicate whether or not a stuffing event occurs in the frame. Both bits shall be set to 1 if the four stuff bits are present at the end of the current frame. Both bits shall be set to 0 if there are no stuff bits at the end of the current frame. In synchronous mode, *sbid1* and *sbid2* are spare bits.

7.1.2.7 *stb1 - stb4* **(Stuffing Bits)**

In plesiochronous mode, these bits are used together. Either zero or four stuffing bits are inserted, depending on the relation of the timing between the upstream and downstream channels. In synchronous framing mode, *stb1* and *stb2* are present in every frame, and *stb3* and *stb4* are not

present. The values of *stb1 - stb4* are specified independently for the upstream and downstream directions.

7.1.3 CRC Generation (*crc1* … *crc6*)

A cyclic redundancy check (CRC) shall be generated for each frame and transmitted on the following frame. The six CRC bits (*crc1* to *crc6*) shall be the coefficients of the remainder polynomial after the message polynomial, multiplied by D^6, is divided by the generating polynomial. The message polynomial shall consist of all bits in the frame except for the synchronization word, CRC bits, and the stuff bits. (There are thus $4k+26$ message bits in a frame that are covered by the CRC check.) The message bits shall be ordered as in the frame itself, i.e. m_0 is the first bit, m_1 is the second bit, etc. The CRC check bits shall be calculated according to the equation:

$$crc(D) = m(D)D^6 \bmod g(D)$$

where:

$$m(D) = m_0 D^{4k+25} \oplus m_1 D^{4k+24} \oplus \ldots \oplus m_{4k+24} D \oplus m_{4k+25}$$

is the message polynomial,

$$g(D) = D^6 \oplus D \oplus 1$$

is the generating polynomial,

$$crc(D) = crc1 D^5 \oplus crc2 D^4 \oplus \ldots \oplus crc5 D \oplus crc6$$

is the CRC check polynomial, $\oplus$ indicates modulo-2 addition (exclusive OR), and D is the delay operator.

7.1.4 Frame Synchronization

In plesiochronous clocking mode, SHDSL uses a variable length PMS-TC frame and bit stuffing to synchronize the PMS-TC frame rate with the incoming payload rate. Quick acquisition of frame synchronization and the ability to maintain frame synchronization in the presence of errors are important properties of the frame structure.

Three types of bit fields are provided for use in frame synchronization: Frame Sync Word, Stuff Bits, and Stuff Bit IDs. The Frame Sync Word is 14 bits long and is present on every frame. The stuff bits are four contiguous bits which are present only at the end of long frames. Stuff Bit Ids are two bits distributed within the frame which indicate whether the current frame contains the four stuffing bits. These distributed bits provide improved immunity to frame alignment errors caused by burst errors.

The precise manner in which this information is used to acquire or maintain frame synchronization is the choice of the receiver designer. Since different frame synchronization algorithms may require different values for the bits of the FSW and Stuff Bits, a provision has been made to allow the receiver to inform the far end transmitter of the particular values that are to be used for these fields in the transmitted PMS-TC frame.

7.1.5 Scrambler

The scrambler in the STU-C and the STU-R transmitters shall operate as shown in Figure 7-1 and Figure 7-2, respectively. In these figures, T_b indicates a delay of one bit duration and $\oplus$ is the binary exclusive-OR operation. The frame sync word bits and the stuff bits in the SHDSL data mode frame (Table 7-1) shall not be scrambled. While the frame sync word bits and stuff bits are present at *f(n)*, the scrambler shall not be clocked, and *f(n)* shall be directly connected to *s(n)*.

7.1.5.1 STU-C Scrambler

The block diagram of the STU-C scrambler is shown in Figure 7-1.

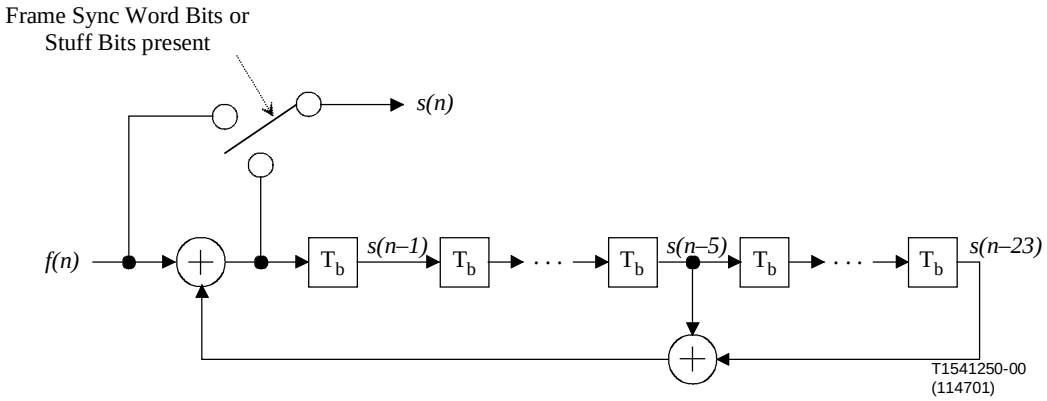


FIGURE 7-1

Block Diagram of the STU-C Scrambler

7.1.5.2 STU-R Scrambler

The block diagram of the STU-R scrambler is shown in Figure 7-2.

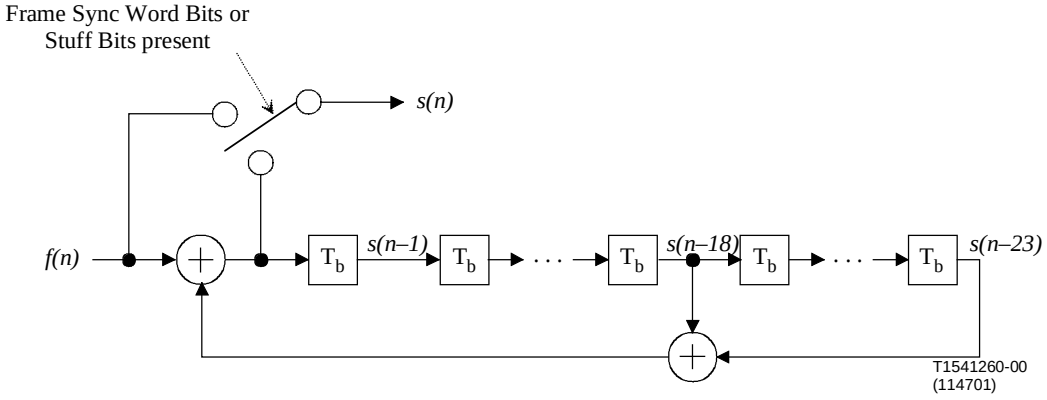


FIGURE 7-2

Block Diagram of the STU-R Scrambler

7.1.6 Differential Delay Buffer

In the optional four-wire mode, it is understood that the characteristics of the two-wire pairs may differ. Differences in wire diameter, insulation type, length, number and length of bridged taps and exposure to impairments may result in differences in transmission time between pairs. It is

recommended that such differences in signal transfer delay between the two pairs be limited to a maximum of 50 µs at 150 kHz, corresponding to about 10 km difference in line length between STU-R and STU-C.

In transceivers supporting four-wire mode, a delay difference buffer shall be implemented to compensate for any difference in total transmission time of the SHDSL frames on different pairs. Such delay differences may be due to the pair differences described above, as well as to delays due to signal processing in the SHDSL transceivers in the STU-C, STU-R and possible signal regenerators. The function of this delay difference buffer is to align the SHDSL frames so that frames can be correctly reassembled. This buffer shall be capable of absorbing a delay difference of at least 6 symbols + 50 µs at the line side of each SHDSL receiver.

7.2 PMS-TC Activation

7.2.1 Activation Frame

The format of the activation frame is shown in Table 7-2. A T_c or T_r signal shall be generated by repetitively applying the activation frame information shown in Table 7-2 to the STU scrambler as shown in Figure 6-5. The activation frame contents shall be constant during the transmission of T_c and T_r. The activation frame sync bits are not scrambled, so they shall be applied directly to the uncoded 2-PAM constellation. The total number of bits in the activation frame is 4227. The activation frame shall be sent starting with bit 1 and ending with bit 4227.

In the optional four-wire mode, activation shall proceed in parallel on each of the two-wire pairs.

TABLE 7-2

Activation Frame Format

Activation Frame Bit LSB:MSB	Definition
1:14	Frame Sync for T_c and T_r: 11111001101011_2, where the left-most bit is sent first in time
	Frame Sync for F_c : 11010110011111_2, where the left-most bit is sent first in time
15:36	Precoder Coefficient 1: 22 bit signed two's complement format with 17 bits after the binary point, where the LSB is sent first in time
37:58	Precoder Coefficient 2
59:3952	Precoder Coefficients 3 – 179
3953:3974	Precoder Coefficient 180
3975:3995	Encoder Coefficient A: 21 bits where the LSB is sent first in time
3996:4016	Encoder Coefficient B: 21 bits where the LSB is sent first in time
4017:4144	Vendor Data: 128 bits of proprietary information
4145:4211	Reserved: 67 bits set to logical zeros
4212:4227	CRC: c_1 sent first in time, c_{16} sent last in time

7.2.1.1 Frame Sync

The frame sync for T_c and T_r is a 14 bit code. In binary, the code shall be 11111001101011, and shall be sent from left to right. For F_c, the frame sync shall be 11010110011111, or the reverse of the frame sync for T_c and T_r.

7.2.1.2 Precoder Coefficients

The precoder coefficients are represented as 22-bit two's complement numbers, with the five most significant bits representing integer numbers from −16 (10000) to +15 (01111), and the remaining 17 bits are the fractional bits. The coefficients are sent sequentially, starting with coefficient C_1 and ending with coefficient C_N (from Figure 6-4), and the least significant bit of each coefficient is sent first in time. The minimum number of precoder coefficients shall be 128 and the maximum number shall be 180. If fewer than 180 precoder coefficients are used, the remaining bits in the field shall be set to zero.

7.2.1.3 Encoder coefficients

Referring to Figure 6-3, the coefficients for the programmable encoder are sent in the following order: a_0 is sent first in time, followed by a_1, a_2, …, and b_{20} is sent last in time.

7.2.1.4 Vendor Data

These 128 bits are reserved for vendor-specific data.

7.2.1.5 Reserved

These 67 bits are reserved for future use and shall be set to logical zeros.

7.2.1.6 CRC

The sixteen CRC bits (c_1 to c_{16}) shall be the coefficients of the remainder polynomial after the message polynomial, multiplied by D^{16}, is divided by the generating polynomial. The message polynomial shall be composed of the bits of the activation frame, where m_0 is bit 15 and m_{4196} is bit 4211 of the activation frame, such that

$$crc(D) = m(D)D^{16} \bmod g(D)$$

where:

$$m(D) = m_0D^{4196} \oplus m_1D^{4195} \oplus \ldots \oplus m_{4195}D \oplus m_{4196}$$

is the message polynomial,

$$g(D) = D^{16} \oplus D^{12} \oplus D^5 \oplus 1$$

is the generating polynomial,

$$crc(D) = c_1D^{15} \oplus c_2D^{14} \oplus \ldots \oplus c_{15}D \oplus c_{16}$$

is the CRC check polynomial, $\oplus$ indicates modulo-2 addition (exclusive OR), and D is the delay operator.

7.2.2 Activation Scrambler

The scrambler in the STU-C and the STU-R transmitters (see Figure 6-5) shall operate as shown in and Figure 7-1 and Figure 7-2, where T_b is a delay of one bit duration, and $\oplus$ is binary exclusive-OR. The frame sync bits in the activation frame shall not be scrambled. While the frame sync bits are present at *f(n)*, the scrambler shall not be clocked, and *f(n)* shall be directly connected to *s(n).*

8 TPS-TC Layer Functional Characteristics

8.1 Payload Block Data Structure

Each Payload Block shall consist of 12 Sub-blocks, and shown in Figure 8-1. The size of each Payload Sub-Block is defined as k_s, where $k_s = i + n\times8$ [bits]. As stated in §7.1, the payload data rate is set by: $n\times64 + i\times8$ kbit/s, where $3 \le n \le 36$ and $0 \le i \le 7$. For n=36, i is restricted to the values of 0 or 1. All structure of data within Payload Sub-Blocks (i.e., support for clear broadband channels, subchannels, and region-specific services) is specified in Annex E.

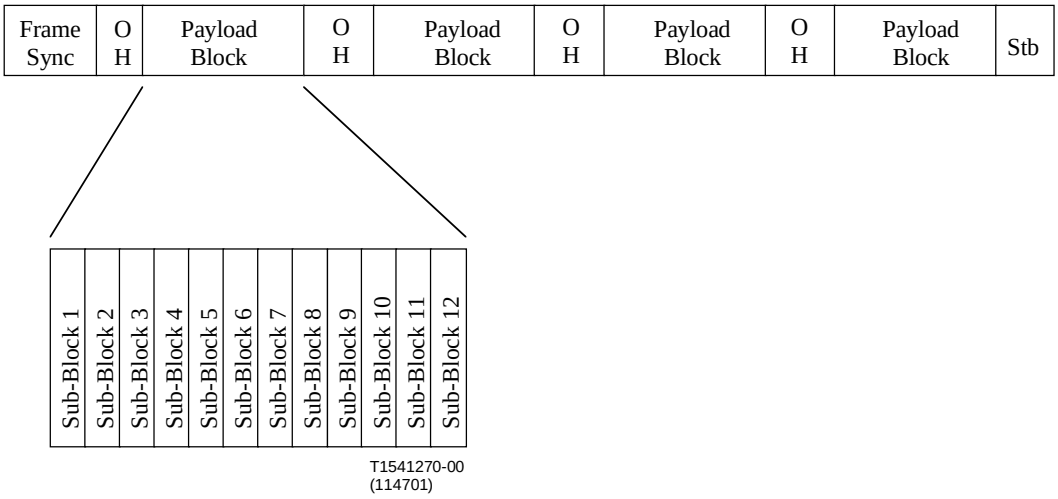


FIGURE 8-1

Structure of Payload Blocks

8.2 Data Interleaving in four-wire Mode

In the optional four-wire mode, interleaving of payload data between pairs is necessary. This shall be accomplished by interleaving within Payload Sub-Blocks between Pair 1 and Pair 2. k_s bits in each Sub-Block shall be carried on Pair 1, and an additional k_s bits shall be carried on Pair 2, as shown in Figure 8-2. The size of each Payload Sub-Block is defined as $2k_s$, where $k_s = i + n\times8$ [bits]. As stated in §7.1, the payload data rate per pair is set by: $n\times64 + i\times8$ kbit/s, where $3 \le n \le 36$ and $0 \le i \le 7$. For n=36, i is restricted to the values of 0 or 1. All structure of data within Payload Sub-Blocks (i.e. support for clear broadband channels, subchannels, and region-specific services) is specified in Annex E.

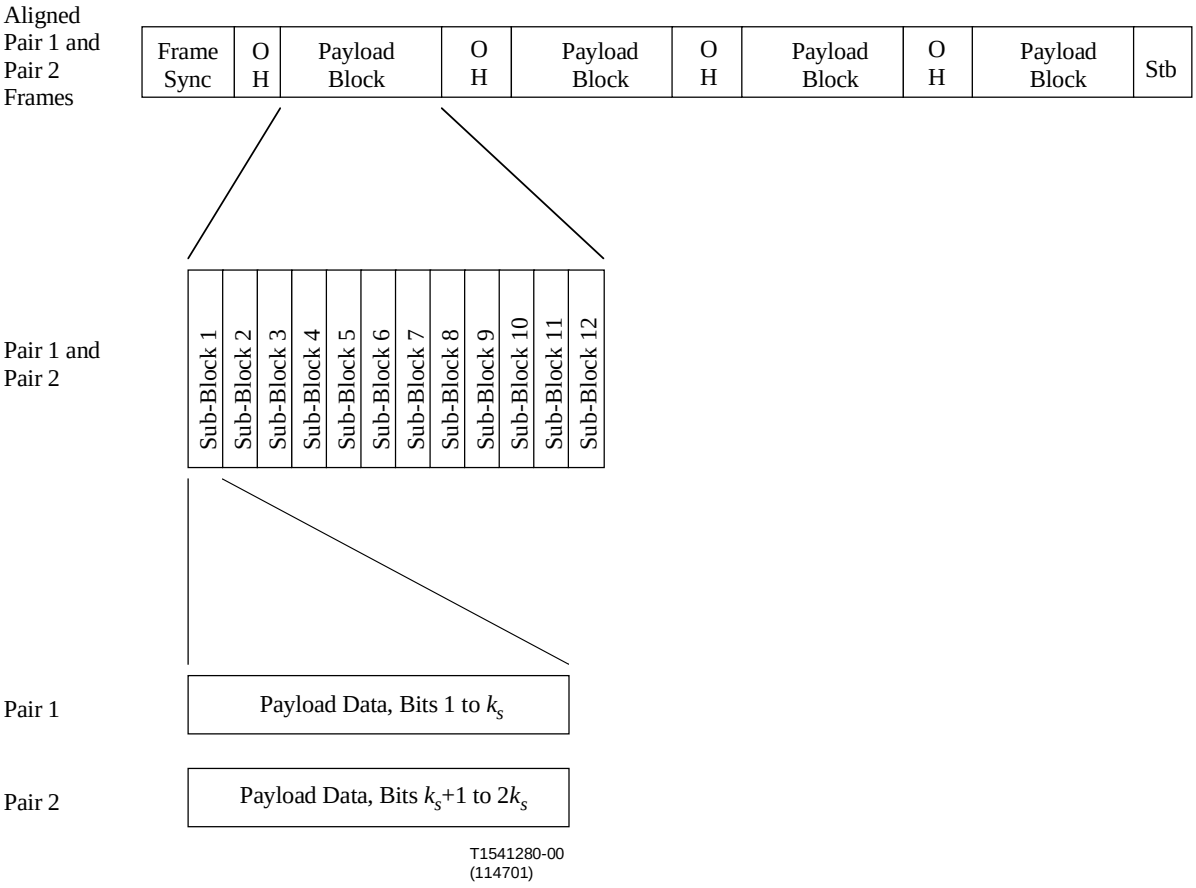
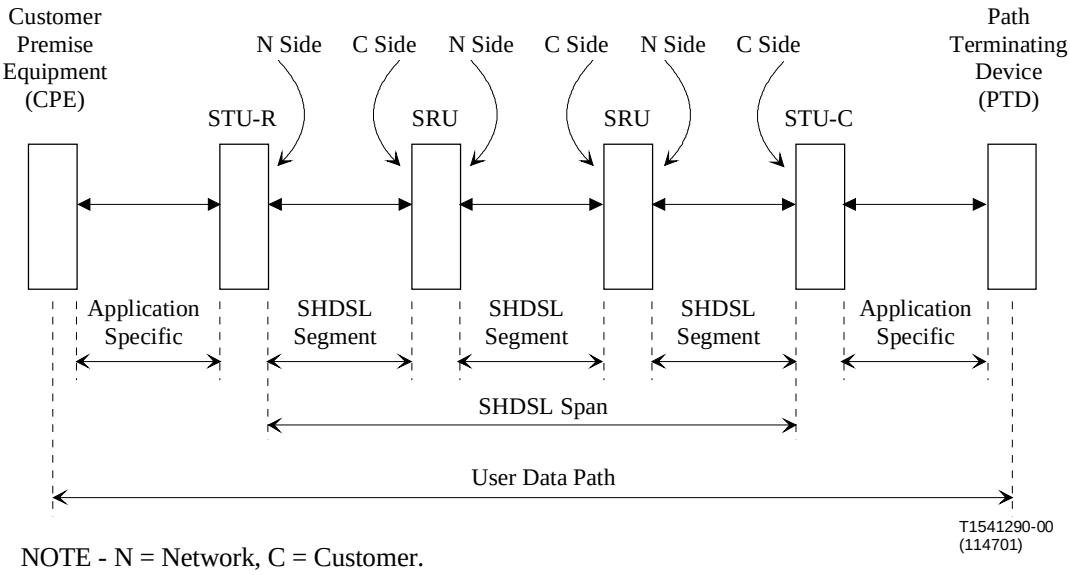


FIGURE 8-2

Data Interleaving within Payload Blocks

9 Management

9.1 Management Reference Model



NOTE - N = Network, C = Customer.

FIGURE 9-1

Management Reference Model

Figure 9-1 shows the Management Reference Model for user data transport over SHDSL. This example includes two regenerator units for informative purposes. The presence of two regenerators is not intended to be a requirement or limit. An SHDSL segment is characterized by a metallic transmission medium utilizing an analogue coding algorithm, which provides both analogue and digital performance monitoring at the segment entity. An SHDSL segment is delimited by its two end points, known as segment terminations. An SHDSL segment termination is the point at which the analogue coding algorithms end and the subsequent digital signal is monitored for integrity.

All SHDSL performance monitoring data is transported over the EOC. The fixed indicator bits in the SHDSL frame are used for rapid communication of interface or SHDSL segment defects, which may lead to protection switching. In addition, the fixed indicator bits may be used for rapid alarm filtering SHDSL segment failures.

9.2 SHDSL Performance Primitives

9.2.1 Cyclical Redundancy Check Anomaly (CRC Anomaly)

A CRC anomaly shall be declared when the CRC bits generated locally on the data in the received SHDSL frame do not match the CRC bits (*crc1 - crc6*) received from the transmitter. A CRC anomaly only pertains to the frame over which it was declared.

9.2.2 Segment Anomaly (SEGA)

An upstream segment anomaly shall be declared when any SRU declares a CRC anomaly for an SHDSL frame moving in the direction from STU-R to STU-C. A downstream segment anomaly

shall be declared when any SRU declares a CRC anomaly for an SHDSL frame moving in the direction from STU-C to STU-R. A segment anomaly indicates that a regenerator operating on a segment has received corrupted data and therefore the regenerated data is unreliable. The purpose of segment anomaly is to ensure internal SHDSL PMD integrity; it is not intended to be reported to an external management entity. A segment anomaly is indicated via the *sega* bit in the SHDSL frame (§ 7.1.2.5.2).

9.2.3 Loss of Sync Defect (LOSW defect)

In plesiochronous mode, an LOSW defect shall be declared when at least three consecutive received frames contain one or more errors in the framing bits. The term framing bits shall refer to that portion of Frame Sync Word, Stuff Bits and Stuff Bit Ids, which are used for frame synchronization. An LOSW defect shall be cleared when at least two consecutive received frames contain no errors in the framing bits.

In synchronous mode, an LOSW defect shall be declared when at least three consecutive received frames contain one or more bit errors in the Frame Sync Word. An LOSW defect shall be cleared when at least two consecutive received frames contain no errors in the Frame Sync Word.

9.2.4 Segment Defect (SEGD)

An upstream segment defect shall be declared when any SRU declares a LOSW defect for data moving in the direction from STU-R to STU-C. A downstream segment defect shall be declared when any SRU declares a LOSW defect for data moving in the direction from STU-C to STU-R. A segment defect indicates that a regenerator has lost SHDSL synchronization and therefore the regenerated data is unavailable. A segment defect shall be cleared when all SRUs have no LOSW defects. This primitive is typically reported to an external management entity and is used to ensure timely protection switching, alarm filtering, etc. A segment defect is indicated via the *segd* bit in the SHDSL frame (§ 7.1.2.5.4).

9.2.5 Loop Attenuation Defect

A Loop Attenuation Defect shall be declared when the observed Loop Attenuation is at a level higher than the configured threshold (§ 9.5.5.7.5).

9.2.6 SNR Margin Defect

An SNR Margin Defect shall be declared when the observed SNR Margin is at a level lower than the configured threshold (§ 9.5.5.7.5). SNR Margin is defined as the maximum dB increase in equalized noise or the maximum dB decrease in equalized signal that a system can tolerate and maintain a BER of 10^{-7}.

9.2.7 Loss of Sync Word Failure (LOSW failure)

An LOSW failure shall be declared after 2.5 ± 0.5 s of contiguous LOSW defect. The LOSW failure shall be cleared when the LOSW defect is absent for 20 s or less (i.e. clear within 20 s). The minimum hold time for indication of LOSW failure shall be 2 s.

9.3 SHDSL Line Related Performance Parameters

9.3.1 Code Violation (CV)

The SHDSL parameter Code Violation is defined as a count of the SHDSL CRC anomalies occurring during the accumulation period. This parameter is subject to inhibiting – see § 9.3.6.

9.3.2 Errored Second (ES)

The SHDSL parameter Errored Second is defined as a count of 1-second intervals during which one or more CRC anomalies are declared and/or one or more LOSW defects are declared. This parameter is subject to inhibiting – see § 9.3.6.

9.3.3 Severely Errored Second (SES)

The SHDSL parameter Severely Errored Second is defined as a count of 1-second intervals during which at least 50 CRC anomalies are declared or one or more LOSW defects are declared. (50 CRC anomalies during a 1-second interval is equivalent to a 30% errored frame rate for a nominal frame length.) This parameter is subject to inhibiting – see § 9.3.6.

9.3.4 LOSW Second (LOSWS)

The SHDSL parameter LOSW Second is defined as a count of 1-second intervals during which one or more SHDSL LOSW defects are declared.

9.3.5 Unavailable Second (UAS)

The SHDSL parameter Unavailable Second is a count of 1-second intervals for which the SHDSL line is unavailable. The SHDSL line becomes unavailable at the onset of 10 contiguous SESs. The 10 SESs are included in the unavailable time. Once unavailable, the SHDSL line becomes available at the onset of 10 contiguous seconds with no SESs. The 10 s with no SESs are excluded from unavailable time.

9.3.6 Inhibiting Rules

- UAS parameter counts shall not be inhibited.

- ES and SES shall be inhibited during UAS. Inhibiting shall be retroactive to the onset of unavailable time and shall end retroactively to the end of unavailable time.

- The CV parameter shall be inhibited during SES.

Further information on inhibiting rules and how ES and SES are decremented can be found in IETF RFC 2495: Definitions of Managed Objects for the DS1, E1, DS2 and E2 Interface Types [B9].

9.4 Performance Data Storage

In order to support SHDSL performance history storage at the STU-C, each SHDSL network element shall monitor performance and maintain a modulo counter for each performance parameter that is specified in § 9.5.5.7.14 and § 9.5.5.7.15, as appropriate. No initialization of these modulo counters is specified or necessary. By comparing the current reading of the modulo counter with the previous reading stored in memory, the data base manager in the STU-C can determine the number of counts to add to the appropriate performance history bin. (Note that the number of counts may decrease under some fault conditions - see § 9.3 for additional information.) The modulo counters are reported in the SHDSL Performance Status Messages (§ 9.5.5.7.14 and § 9.5.5.7.15).

The STU-C shall collect performance history by polling each SHDSL network element with a time interval that precludes overflow of the modulo counter. For example, the modulo counter for Errored Seconds is 8 bits which allows a maximum of 255 s between polls before overflow may occur. Note that the polling that is referred to herein is implemented by the internal data base manager in the STU-C rather than an external network manager.

The STU-C shall maintain performance history bins for each SHDSL segment endpoint. The performance history bins shall include the total collected counts for the current 15 minute period, 32 previous 15 minute periods, current 24 hour period, and 7 previous 24 hour periods.

9.5 Embedded Operations Channel

9.5.1 Management Reference Model

The STU-C shall maintain a management information database for external access by network management or via craft interface.

Optionally, the STU-R may maintain a management information database, which can be locally accessed (through a craft interface). This is particularly useful when the STU-C, due to fault conditions, is unreachable via the EOC.

Access to the management information database from craft interfaces on attached units shall be provided through a virtual-terminal interface.

9.5.2 EOC Overview and Reference Model

The EOC allows terminal units to maintain information about the span. There are two basic flows of data, differentiated by which terminal unit initiates the data flow (and subsequently stores the information for external access). The data flow initiating from the STU-C is mandatory. The data flow initiating from the STU-R is optional, but all units must respond to requests in either direction of data flow. In all cases the "master database" shall be stored at the STU-C and all conflicts shall be resolved in favour of the STU-C (i.e. the information at the STU-C takes precedence). The data flows are illustrated in Table 9-1 for a two regenerator link (Q denotes a query or command message, R denotes a response message). Up to eight regenerators are supported by the protocol definition. Asterisks denote optional message transmissions. A block diagram example of a link with two regenerators is shown in Figure 9-1.

TABLE 9-1

Illustration of EOC Flow with Two Regenerators

Messages from STU-C Msg(src,dest)	**Messages from SRU1 Msg(src,dest)**	**Messages from SRU2 Msg(src,dest)**	**Messages from STU-R Msg(src,dest)**
Q(1,3) →	→ Process		
Process ←	← R(3,1)		
Q(1,4) →	→ Forward →	→ Process	
Process ←	← Forward ←	← R(4,1)	
Q(1,2) →	→ Forward →	→ Forward →	→ Process
Process ←	← Forward ←	← Forward ←	←R(2,1)
		Process ←	←Q(2,3)*
		R(3,2) →	→ Process
	Process ←	← Forward ←	←Q(2,4)*
	R(4,2) →	→ Forward →	→ Process
Process ←	← Forward ←	← Forward ←	←Q(2,1)*
R(1,2) →	→ Forward →	→ Forward →	→ Process
* indicates optional messages			

The data link layer of SHDSL EOC checks the FCS and if valid passes the packet to the network layer. If the CRC is invalid the entire packet is ignored. The network layer consists of three possible actions: Process, Forward, and Ignore/Terminate. Process means that the source address and HDLC information field are passed on to the application layer. Forward means that the packet is sent onward to the next SHDSL element. (Note that only SRUs will forward packets.) Ignore/Terminate means that the HDLC packet is ignored and is not forwarded. An SRU may both process and forward a packet in the case of a broadcast message. If the segment is not active in the forwarding direction, the SRU shall discard the packet instead. When the segment is active in the forwarding direction, the maximum forwarding delay in an SRU shall be 300 ms. All retransmission and flow control is administered by the endpoints, the STUs.

To accommodate the dual data flows, SHDSL regenerators have dual addresses as shown in Table 9-1. One address is for communication with the STU-C and the other address is for communication with the STU-R. During Discovery, the STU-C and optionally the STU-R send discovery probe messages, which propagate across the span and allow the SRUs to be numbered via a hop count field in the message. This process is explained in detail below.

The SHDSL terminal units communicate unidirectionally and thus have only one address. The STU-C is assigned a fixed address of 1 and the STU-R is assigned a fixed address of 2. At power-up, each SRU is assigned the address of 0 for each direction. Under a LOSW failure condition, the SRU shall reset its source address to 0 for the direction in which the LOSW failure exists. The SRU source address shall be changed from 0 if and only if a discovery probe message is received and processed. In this way, a regenerator will only communicate in the direction of a database. For instance, if a regenerator receives a probe message from the STU-C and not from the STU-R then its address will remain 0 in the direction towards the remote.

9.5.3 EOC Startup

After loop activation, the SHDSL EOC goes through three initialization stages: Discovery, Inventory and Configuration. During Discovery, the STU-C and optionally the STU-R will learn if any mid-span regenerators exist and their addresses will be determined. During Inventory, the STU-C will poll each SRU and the STU-R to establish inventory information on each element for the terminal unit's database. (Similarly, the STU-R may poll each SRU and the STU-C to establish its own database, although this is optional.) During Configuration, the STU-C configures the STU-R and any SRUs for alarm thresholds, signal characteristics, etc. There is no enforcement of the order or time of the Inventory and Configuration phases; the initiating STU is in control.

The following table is an example of Discovery starting from the STU-C and then followed by an optional Discovery initiated by the STU-R. Although these are shown sequentially in this example, they are actually independent; it is not necessary for the STU-R to wait until it received the probe from the STU-C before initiating its own Discovery phase. The STU-R may send its probe as soon as its EOC is active. The Discovery Response contains the current hop count, the vendor ID, EOC version and an indication of LOSW in the forward direction (i.e. in the direction of EOC flow that is opposite to the direction that the Discovery Response is sent).

TABLE 9-2

Illustration of EOC Discovery Phase

Messages from STU-C Msg(src,dest,h)	**Messages from SRU1 Msg(src,dest,h)**	**Messages from SRU2 Msg(src,dest,h)**	**Messages from STU-R Msg(src,dest,h)**
DP(1,0,0)→			
	← DR(3,1,1)		
	DP(0,0,1)→		
	←Forward ←	← DR(4,1,2)	
		DP(0,0,2)→	
	←Forward ←	←Forward ←	← DR(2,1,3)
			← DP(2,0,0)
		DR(3,2,1)→	
		← DP(4,0,1)	
	DR(4,2,2)→	→Forward →	
	← DP(3,0,2)		
DR(1,2,3) →	→Forward →	→Forward →	
NOTE - h = hop count, DP = Discovery Probe, DR = Discovery Response			

After the Initiator (STU-C and optionally STU-R) has received a Discovery Response message from an element, it shall then begin the Inventory phase for that particular element. This is accomplished by polling that particular element for its inventory information. After the Initiator has received the inventory information for a unit, it shall then begin the Configuration phase by sending the appropriate configuration information to the corresponding element. The Inventory and Configuration Phases operate independently for each responding terminal/regenerator unit.

To ensure interoperability, the behavior of slave or responding units is carefully specified by this Recommendation. The particular method for handling dropped packets or no response is left to the discretion of the initiating STU.

Table 9-3 shows the EOC state table for the network side of an SRU. Note that an identical, but independent, state machine exists for the customer side of an SRU to support messages originating from the STU-R.

The state machine consists of three states: Offline, Discovery and EOC Online. The Offline state is characterized by LOSW failure (a loss of SHDSL sync). The Discovery state is characterized by an unknown address. Once the address is learned through the Discovery message, the SRU enters the EOC online or active state. At this point, the SRU will respond to inventory, configuration, maintenance, or other messages from the STU-C.

TABLE 9-3

SRU Network EOC State Table

Offline State

Event	Action
Network LOSW = 0	EOC State = Discovery Ready;

Discovery Ready State

Event	Action
Network LOSW = 1	Network EOC Address = 0; Network EOC State = Offline;
Discovery probe message received from the Network side	Increment Hop Count Set Network EOC address to Hop Count + 2; Compose and present Discovery message to Customer side application layer; Send Discovery Response to STU-C; Network EOC State = EOC Online;
Message with address not equal to unit's address received from the Network side.	Request forwarding of the message from the Customer side network layer;
Message Forwarding Requested from Customer side	Send requested message toward Network if EOC not offline;

EOC Online State

Event	Action
Network LOSW = 1	Network EOC Address = 0; Network EOC State = Offline;
Discovery message received from the Network side	Increment Hop Count Set Network EOC address to Hop Count + 2; Compose and present Discovery message to Customer side application layer; Send Discovery Response to STU-C;
Message with broadcast destination address received from the Network side	Process the message; Request the Customer side EOC network layer to forward the message;
Message with unit's destination address or address 0 received from the Network side	Process the message;
Message with address not equal to unit's address received from the Network side	Request forwarding of message from the Customer side network layer;
Message forwarding requested from Customer side network layer	Send requested message toward Network if EOC not offline;

9.5.4 Remote Management Access

The STU-C shall maintain the master management database for the entire SHDSL span. (An optional second database is maintained at the STU-R.) Other units are only required to store enough information to accurately send information via the EOC. The information contained in the master database shall be accessible from any SHDSL unit that has a craft port and from network management if it is available. The craft access is in the form of a virtual-terminal interface (or virtual-craft-port interface). This interface is defined so that it can be used by any attached unit to access the terminal screen of another unit on the same SHDSL span. Support for this feature is

optional, with the exception of the STU-C, which shall support the "host" side of at least one remote terminal connection. (Whether this interface can be active simultaneously with local craft access to the STU-C is a vendor decision and beyond the scope of this Recommendation.) The virtual-terminal interface consists of connect, disconnect, keyboard, and screen messages. After a connection has been established, input characters from the craft port are sent in Keyboard data messages to the "host" unit. The host unit, in turn, shall send information in the form of ASCII text, ASCII control codes, and screen control functions in Screen messages, whose contents are transmitted back to the craft port. The host unit shall echo characters.

The method for determining that remote access through the local craft port is desired or should be terminated is vendor specific, and beyond the scope of this Recommendation. Whatever method is used, capability for transmitting all valid key sequences (ASCII characters and control codes) shall be provided.

9.5.5 EOC Transport

The EOC shall be transported in the SHDSL frame in bits *eoc1* through *eoc20*. Five octets are contained in each two SHDSL frames, with specified alignment. The least significant bit (LSB) of the octets are located in bits 1, 9, and 17 of the EOC bits in the first frame and bits 5 and 13 of the second frame; each octet is transmitted LSB first. Octet alignment across frames is achieved through detection of the alignment of the HDLC Sync pattern ($7E_{16}$).

For optional dual loop operation, each EOC message shall be sent in parallel such that redundant and identical messages are sent over both loops.

9.5.5.1 EOC Data Format

Numerical data and strings are placed in the EOC with octet alignment. Data items that are not an integral number of octets have been packed together to minimize message sizes.

Numerical Fields shall be transmitted most significant octet first, least significant bit first within an octet. (This is consistent with "network octet ordering" as in IETF RFC 1662: PPP in HDLC-like Framing [4].)

Strings shall be represented in the data stream with their first character (octet) transmitted first. Strings shall be padded with spaces or terminated with a NULL (00_{16}) to fill the allocated field size. String fields are fixed length so characters after a NULL in a string data field are "don't care".

9.5.5.2 EOC Frame Format

The EOC channel shall carry messages in an HDLC-like format as defined in ITU-T G.997.1, § 6.2 [3]. The channel shall be treated as a stream of octets; all messages shall be an integral number of octets.

The frame format uses a compressed form of the HDLC header, as illustrated in Table 9-4. The destination address field shall be the least significant 4 bits of octet 1; the source address field shall occupy the most significant 4 bits of the same octet (the address field). There is no control field. One or more sync octets ($7E_{16}$) shall be present between each frame. Inter-frame fill shall be accomplished by inserting sync octets as needed. Discovery probe messages shall be preceded by at least 5 sync octets to assure proper detection of octet alignment. The Information Field contains exactly one Message as defined below. The maximum length of a frame shall be 75 octets, not including the sync pattern or any octets inserted for data transparency.

TABLE 9-4

Frame Format for SHDSL EOC

	MSB	LSB	
Octet #	Contents		
	Sync pattern $7E_{16}$		
	Source address bits 7..4	Destination address bits 3..0	
1	Message ID per Table 9-6.		Information
2	Message Content - Octet 2		Field
	…		…
L	Message Content - Octet L		…
	FCS octet 1		
	FCS octet 2		
	Sync pattern $7E_{16}$		

9.5.5.3 Data Transparency

Transparency for the information payload to the sync pattern ($7E_{16}$) and the control escape pattern $7D_{16}$ shall be achieved by octet stuffing.

Before transmission:

- octet pattern $7E_{16}$ is encoded as two octets $7D_{16}$, $5E_{16}$;
- octet pattern $7D_{16}$ is encoded as two octets $7D_{16}$, $5D_{16}$.

At reception:

- octet sequence $7D_{16}$, $5E_{16}$ is replaced by octet $7E_{16}$;
- octet sequence $7D_{16}$, $5D_{16}$ is replaced by octet $7D_{16}$;
- any other two-octet sequence beginning with $7D_{16}$ aborts the frame.

9.5.5.4 Frame Check Sequence

The frame check sequence (FCS) shall be calculated as specified in IETF RFC 1662 [4]. (Note that the FCS is calculated before data transparency.) The FCS shall be transmitted as specified in IETF RFC 1662: Bit 1 of the first octet is the MSB and bit 8 of the second octet is the LSB, i.e. the FCS bits are transmitted reversed from the normal order.

9.5.5.5 Unit Addresses

Each unit uses one source and destination address when communicating with upstream units and a separate, independent source and destination address when communicating with downstream units. Each address shall have a value between 0_{16} and F_{16}. Units shall be addressed in accordance with Table 9-5. Address F_{16} may only be used as a destination address and shall specify that the message is addressed to all units. Address 0_{16} is used to address the next attached or adjacent unit.

TABLE 9-5

Device Addresses

Address ($Base_{16}$)	Device
0	adjacent device
1	STU-C
2	STU-R
3 - A	Regenerators 1 - 8
B - E	Reserved (D and E not allowed)
F	Broadcast message, to all stations

NOTE - This Recommendation is not intended to indicate how many regenerators can or should be supported by a product; only how to identify them if they exist.

9.5.5.6 Message IDs

Table 9-6 summarizes message ID. Message IDs are listed as decimal numbers. Messages 0-64 represent request messages. Messages 128-192 represent messages that are sent in response to request messages. Each request message is acknowledged with the corresponding response. Request/Response Message IDs usually differ by an offset of 128.

TABLE 9-6

Summary of Message IDs

Message ID(decimal)	Message Type	Initiating Unit	Reference
0	Reserved		
1	Discovery Probe	STU-C, STU-R*, SRU	§ 9.5.5.7.1
2	Inventory Request	STU-C, STU-R*	§ 9.5.5.7.3
3	Configuration Request – SHDSL	STU-C	§ 9.5.5.7.5
4	Reserved for Application Interface Configuration		
5	Configuration Request – Loopback Timeout	STU-C, STU-R*	§ 9.5.5.7.6
6	Virtual Term. Connect Req.	STU-R*, SRU*	§ 9.5.5.7.16
7	Virtual Terminal Disc. Req.	STU-R*, SRU*	§ 9.5.5.7.16
8	Keyboard data message	STU-R*, SRU*	§ 9.5.5.7.17
9	Maintenance request – System Loopback	STU-C, STU-R*	§ 9.5.5.7.18
10	Maintenance request – Element Loopback	STU-C, STU-R*	§ 9.5.5.7.19
11	Status Request	STU-C, STU-R*	§ 9.5.5.7.11
12	Full Status Request	STU-C, STU-R*	§ 9.5.5.7.12
13-14	Reserved		

15	Soft restart/Power backoff disable Request	STU-C	§ 9.5.5.7.21
16	Reserved (Future)		
17	ATM Cell Status Request	STU-C, STU-R*	§ E.9.4.7
18	STU-R Configuration Request – Management	STU-C	§ 9.5.5.7.9
19	Reserved for Voice Transport Request (Future)	Undefined	
20	ISDN Request	STU-C, STU-R	§ E.8.7.1
21-63	Reserved (Future)		
64-88	Reserved for Line management Request	Undefined	§ 9.5.5.7.22
89-111	Reserved		
112-119	Proprietary Message	Undefined	§ 9.5.5.7.23
120	External Message	Undefined	§ 9.5.5.7.24
121	G.997.1 Message	STU-C*, STU-R*	§ 9.5.5.7.25
122-124	Reserved		
125-127	Excluded ($7D_{16}$, $7E_{16}$, $7F_{16}$)		
128	Reserved		
129	Discovery Response	All	§ 9.5.5.7.2
130	Inventory Response	All	§ 9.5.5.7.4
131	Configuration Response - SHDSL	STU-R, SRU	§ 9.5.5.7.7
132	Reserved for Application Interface Configuration		
133	Configuration Response - Loopback Timeout	All	§ 9.5.5.7.8
134	Virtual Terminal Connect Response	STU-C, SRU*, STU-R*	§ 9.5.5.7.16
135	Reserved		
136	Screen data message	STU-C, SRU*, STU-R*	§ 9.5.5.7.17
137	Maintenance Status	All	§ 9.5.5.7.20
138	Reserved		
139	Status /SNR	All	§ 9.5.5.7.13
140	Performance Status SHDSL Network Side	SRU, STU-R	§ 9.5.5.7.14
141	Performance Status SHDSL Customer Side	STU-C, SRU	§ 9.5.5.7.15
142	Reserved for Application Interface Performance		
143	Reserved (Future)		
144	Generic Unable to Comply (UTC)		§ 9.5.5.7.26
145	ATM Cell Status Information	All	§ E.9.4.8

146	Configuration Response - Management	STU-R, SRU	§ 9.5.5.7.10
147	Reserved for Voice Transport Response (Future)	Undefined	
148	ISDN Response	STU-C, STU-R	§ E.8.7.1
149-191	Reserved (Future)		
192-216	Segment Management Response (reserved)	Undefined	§ 9.5.5.7.22
217-239	Reserved (Future)		
240-247	Proprietary message Response	Undefined	§ 9.5.5.7.23
248-252	Reserved		
253-255	Excluded (FD_{16}, FE_{16}, FF_{16})		
NOTE - *Denotes optional support. A unit may initiate this message.			

9.5.5.7 Message Contents

Each message shall have the contents in the format specified in Table 9-7 through Table 9-31. If any message has a message length longer than expected and is received in a frame with a valid FCS, then the known portion of the message shall be used and the extra octets discarded. This will permit addition of new fields to existing messages and maintain backward compatibility. New data fields shall only be placed in reserved bits after the last previously defined data octet. Reserved bits and octets shall be filled with the value 00_{16} for forward compatibility.

Response messages may indicate UTC (Unable to Comply). Note that this is not an indication of non-compliance. UTC indicates that the responding unit was unable to implement the request.

9.5.5.7.1 Discovery Probe - Message ID 1

The Discovery Probe message shall be assigned Message ID 1, and is used to allow an STU to determine how many devices are present and assign addresses to those units.

TABLE 9-7

Discovery Probe Information Field

Octet #	Contents	Data Type	Reference
1	1	Message ID	
2	Hop Count	unsigned char	§ 9.5.3

9.5.5.7.2 Discovery Response – Message ID 129

The Discovery Response message shall be assigned Message ID 129. This message shall be sent in response to a Discovery Probe Message. The Hop Count field shall be set to 1 larger than the value received in the Discovery Probe Message causing the response. (The Full Receive State Machine is described in Table 9-3.) Forward LOSW indication means that the segment is down in the forward direction from the SRU. In the case of two loop operation, Forward LOSW indication means that both loops are down in the forward direction from the SRU. In either case, the SRU is unable to forward the Discovery Probe message to the adjacent unit and it reports this fact to the initiating STU. The Forward LOSW octet field shall be set to 00_{16} for responses from an STU.

TABLE 9-8

Discovery Response Information Field

Octet #	Contents	Data Type	Reference
1	129	Message ID	
2	Hop Count	unsigned char	§ 9.5.3
3	Reserved		
4-11	Vendor ID (ordered identically to bits in G.994.1 Vendor ID)		
12	Vendor EOC Software Version	unsigned char	
13	SHDSL Version #	unsigned char	
14 bit 7..1	Reserved		
14 bit 0	Forward LOSW indication, EOC unavailable	Bit	1 = Unavailable 0 = Available

9.5.5.7.3 Inventory Request - Message ID 2

The Inventory Request message shall be assigned Message ID 2. This message is used to request an Inventory Response from a particular unit. It shall only be transmitted by STU devices. There shall be no octets of content for this message.

TABLE 9-9

Inventory Request Information Field

Octet #	Contents	Data Type	Reference
1	2	Message ID	

9.5.5.7.4 Inventory Response - Message ID 130

The Inventory Response message shall be assigned Message ID 130. This message shall be sent in response to an Inventory Request Message.

TABLE 9-10

Inventory Response Information Field

Octet #	Contents	Data Type	Reference
1	130	Message ID	
2	SHDSL Version #	unsigned char	
3-5	Vendor List #	3 octet string	
6-7	Vendor Issue #	2 octet string	
8-13	Vendor Software Version	6 octet string	
14-23	Unit Identification Code (CLEI™)	10 octet string	
24	Reserved		
25-32	Vendor ID (ordered identically to bits		

	in G.994.1 Vendor ID)		
33-44	Vendor model #	12 octet string	
45-56	Vendor serial #	12 octet string	
57-68	Other vendor information	12 octet string	

9.5.5.7.5 Configuration Request - SHDSL: Message ID 3

The Configuration Request - SHDSL message is transmitted by the STU-C to configure the SHDSL interface(s) of attached units. This message may be broadcast or addressed to specific units. It is acknowledged with a Configuration Response - SHDSL message. For SHDSL, SNR is measured internal to the transceiver decision device as opposed to the external segment termination. The "Off" setting indicates that threshold crossings are not reported. Loop Attenuation and SNR Margin are local alarms that are reported in Messages 140 and 141. In addition, these alarms may be physically indicated on the equipment. SHDSL Loop Attenuation shall be defined as follows:

$$LoopAtten_{SHDSL}(H) = \frac{2}{f_{sym}} \left(\begin{array}{c} \int_0^{\frac{f_{sym}}{2}} 10 * \log_{10} \left[\sum_{n=0}^{1} S(f - nf_{sym}) \right] df - \\ \int_0^{\frac{f_{sym}}{2}} 10 * \log_{10} \left[\sum_{n=0}^{1} S(f - nf_{sym}) \left| H(f - nf_{sym}) \right|^2 \right] df \end{array} \right)$$

where f_{sym} is the symbol rate, $\frac{1}{H(f)}$ is the insertion loss of the loop, and $S(f)$ is the nominal transmit PSD.

TABLE 9-11

Configuration Request – SHDSL Information Field

Octet #	Contents	Data Type	Reference
1	3	Message ID	
2 bit 7	Config Type	Bit	0-normal, 1-Read only
2 bits 6..0	SHDSL Loop Attenuation threshold (dB)	Enumerated	0 = off, 1 to 127
3 bits 7..4	SHDSL SNR Margin threshold (dB)	Enumerated	0 = off, 1 to 15
3 bits 3..0	Reserved		set to 0

9.5.5.7.6 Configuration Request - Loopback Timeout: Message ID 5

The Configuration Request - Loopback Timeout message is transmitted by the STU-C (and optionally the STU-R) to set loopback timeouts for individual elements. If a loopback is not cleared before the expiration of the timeout, then the element shall revert to normal operation. This message may be broadcast or addressed to specific units. It is acknowledged with a Configure Response - Loopback Timeout message. If date and time information is sent in octets 4-21, then these strings shall conform to ISO 8601 [5]. If date and time information is not sent, then these fields shall be filled with zeros.

TABLE 9-12

Configuration Request - Loopback Timeout Information Field

Octet #	Contents	Data Type	Reference
1	5	Message ID	
2 bit 7	Config Type	Bit	0 = normal, 1 = Read-only.
2 bits 6..4	Reserved		
2 bits 3..0-3	Loopback timeout	12-bit unsigned integer	In minutes, 0 = no timeout
4-13	YYYY-MM-DD	10 octet date string	ISO 8601 [5]
14-21	HH:MM:SS	8 octet time string	ISO 8601

9.5.5.7.7 Configuration Response - SHDSL: Message ID 131

The Configuration Response - SHDSL message is transmitted to the STU-C in response to a Configuration Request - SHDSL message. This response is sent after the applicable configuration changes have been made. The values of the response shall be set to the new values, after they have been applied. If a transceiver unit is unable to comply with the request, the bit in the Compliance Octet is set and the current settings are reported. If the Config Request message was received with a Config Type of "Read-Only," then no changes are made to the current configuration and the current values are reported.

TABLE 9-13

Configuration Response - SHDSL Information Field

Octet #	Contents	Data Type	Reference
1	131	Message ID	
2 bits 7..1	Reserved		
2 bit 0	UTC (Unable to Comply)	Bit	0 = OK, 1 = UTC
3	SHDSL Loop Attenuation threshold (dB)	Char	0 = off, 1 to 127
4 bits 7..4	SHDSL SNR Margin threshold (dB)	Enumerated	0 = off, 1 to 15
4 bits 3..0	Reserved		set to 0

9.5.5.7.8 Configuration Response - Loopback Timeout: Message ID 133

The Configuration Response - Loopback Timeout message is transmitted to acknowledge the Configuration Request - Loopback Timeout message. This response is sent after the applicable configuration changes have been made. The values of the response shall be set to the new values, after they have been applied. If a transceiver unit is unable to comply with the request, the bit in the Compliance Octet is set and the current settings are reported. If the Config Request message was received with a Config Type of "Read-Only," then no changes are made to the current configuration and the current values are reported.

TABLE 9-14

System Loopback Timeout Response Information Field

Octet #	Information Field	Data Type	Reference
1	133	Message ID	
2 bits 7..1	Reserved		
2 bit 0	UTC (Unable to Comply)	bit	0 = OK, 1 = UTC
3 bits 7..4	Reserved		
3 bits 3..0 - 4	Loopback timeout	12-bit unsigned integer	In minutes, 0 = no timeout
5-14	YYYY-MM-DD	10 octet date string	ISO 8601 [5]
15-22	HH:MM:SS	8 octet time string	ISO 8601

9.5.5.7.9 STU-R Config - Management: Message ID 18

The Config Request - Management message is transmitted by the STU-C to enable or disable STU-R initiated management flow. The destination address shall be F_{16} to indicate this is a broadcast message. STU-R Initiated Management Flow is enabled by default. When disabled, an SRU shall not respond to any STU-R-initiated Request messages, and the STU-R shall not issue any such messages (messages 2-12).Config Type of Read-Only indicates that the addressed unit ignore the subsequent values in the message and report back its current configuration.

TABLE 9-14A

Configuration Request – Management Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 18	Message ID	
2 Bit 7	ConfigType	bit	0-normal, 1-Read-Only
2 Bits 6..1	Reserved		
2 Bit 0	STU-R Initiated Management Flow	bit	0-Enable, 1-Disabled

9.5.5.7.10 Config Response - Management message: Message ID 146

Config Response - Management message is sent by all units to acknowledge to the Config Request - Management message.

TABLE 9-14B

Configuration Response – Management Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 146	Message ID	
2 Bits 7..1	Reserved		
2 Bit 0	UTC (Unable to Comply)	bit	0-OK, 1-UTC
3 Bits 7..1	Reserved		
3 Bit 0	STU-R Initiated Management Flow Status	bit	0-Enabled, 1-Disabled

9.5.5.7.11 Status Request - Message ID 11

The Status Request message is used to poll an element for alarm and general performance status.

The polled unit will respond with one or more of the following status response messages:

- Status/SNR Response - 139 (§ 9.5.5.7.13).
- SHDSL Network Side Performance Status - 140 (§ 9.5.5.7.14).
- SHDSL Customer Side Performance Status - 141 (§ 9.5.5.7.15).
- Maintenance Status - 137 (§ 9.5.5.7.20).

In the optional two-pair mode, messages 139, 140, and 141 contain status information that is specific to a particular pair. In this case, two messages each (one corresponding to each pair) of types 139, 140, and 141 may be sent by the polled unit in response to a status request message.

If active alarm, fault or maintenance conditions exist then the polled unit shall respond with the messages that correspond to the active conditions.

If there has been any change in performance status other than SNR Margin since the last time a unit was polled then the unit shall respond with the messages which contain the change in performance status.

Otherwise, the polled unit shall respond with the Status/SNR Response - 139 (§ 9.5.5.7.13).

TABLE 9-15

Status Request Information Field

Octet #	Information Field	Data Type
1	Message ID 11	Message ID

9.5.5.7.12 Full Status Request - Message ID 12

The Full Status Request message is used to poll an element for its complete current status. The following messages shall be sent in response to the Full Status Request:

- SHDSL Network Side Performance Status (§ 9.5.5.7.14).
- SHDSL Customer Side Performance Status (§ 9.5.5.7.15).
- Maintenance Status (§ 9.5.5.7.20).

In the optional two-pair mode, the following messages shall be sent in response to the Full Status Request:

- SHDSL Network Side Performance Status (§ 9.5.5.7.14) - related to Loop 1.
- SHDSL Network Side Performance Status - related to Loop 2.
- SHDSL Customer Side Performance Status (§ 9.5.5.7.15) - related to Loop 1.
- SHDSL Customer Side Performance Status - related to Loop 2.
- Maintenance Status (§ 9.5.5.7.20).

TABLE 9-16

Full Status Request Information Field

Octet #	Information Field	Data Type
1	Message ID 12	Message ID

9.5.5.7.13 Status Response/SNR - Message ID 139

The Performance Status/SNR message shall be sent in response to the Status Request message under the conditions specified in § 9.5.5.7.9. The reported integer represents dB SNR Noise Margin values rounded up. Because each STU only connects to one SHDSL segment, the application interface side SNR margin data shall be 0 (i.e. the Network Side SNR Margin shall be 0 at the STU-C and the Customer Side SNR shall be 0 at the STU-R).

TABLE 9-17

Status Response OK/SNR Information Field

Octet #	Information Field	Data Type
1	Message ID 139	Message ID
2	Network Side SNR Margin (dB)	signed char (127 = Not Available)
3	Customer Side SNR Margin (dB)	signed char (127 = Not Available)
4	Loop ID	unsigned char (1 = Loop 1, 2 = Loop 2)

9.5.5.7.14 SHDSL Network Side Performance Status - Message ID 140

This message provides the SHDSL Network Side Performance Status. Device Fault shall be used to indicate hardware or software problems on the addressed unit. The definition of Device Fault is vendor dependent but is intended to indicate diagnostic or self-test results. DC Continuity Fault shall be used to indicate conditions that interfere with span powering such as short and open circuits. The definition of DC Continuity Fault is vendor dependent.

In octet 11, bits 7..4 are used to indicate that an overflow or reset has occurred in one or more of the modulo counters. Bits 7 and 5 shall indicate that an overflow has occurred since the last SHDSL Network Side status response. For example, if more than 256 Errored Seconds occur between SHDSL Network Side status responses, then the ES modulo counter will overflow. Bits 6 and 4 shall be used to indicate that one or more of the modulo counters have been reset for any reason (e.g. system powerup or a non service-affecting reset.) Bits 7 and 6 shall be cleared to 0 after a SHDSL Network Side status response is sent to the STU-C. Bits 5 and 4 shall be cleared to 0 after a SHDSL Network Side status response is sent to the STU-R.

TABLE 9-18

SHDSL-Network Side Performance Status Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 140	Message ID	
2 bit 7	Reserved		
Bit 6	N - Power Backoff Status	bit	0 = default 1 = selected
Bit 5	Device Fault	bit	0 = OK, 1 = Fault
Bit 4	N - DC Continuity Fault	bit	0 = OK, 1 = Fault
Bit 3	N - SNR Margin alarm	bit	0 = OK, 1 = alarm
Bit 2	N - Loop Attenuation Alarm	bit	0 = OK, 1 = alarm
Bit 1	N - SHDSL LOSW Failure Alarm	bit	0 = OK, 1 = alarm
Bit 0	Reserved		set to 0
3	N - SHDSL SNR Margin (dB)	signed char (127 = NA)	
4	N - SHDSL Loop Attenuation (dB)	signed char (–128 = NA)	
5	N - SHDSL ES Count modulo 256	unsigned char	
6	N - SHDSL SES Count modulo 256	unsigned char	
7-8	N - SHDSL CRC Anomaly Count modulo 65,536	unsigned int	
9	N - SHDSL LOSW Defect Second Count modulo 256	unsigned char	
10	N - SHDSL UAS Count modulo 256	unsigned char	
11 bit 7	N - Counter Overflow Indication to STU-C		0 = OK 1 = Overflow
11 bit 6	N - Counter Reset Indication to STU-C		0 = OK 1 = Reset
11 bit 5	N - Counter Overflow Indication to STU-R		0 = OK 1 = Overflow
11 bit 4	N - Counter Reset Indication to STU-R		0 = OK 1 = Reset
11 bits 3 ..0	N-Power Back-Off Base Value (dB)	unsigned char	0 .. 15
12 bit 7	N-Power Back-Off Extension (dB)	bit	0→ PBO = Base Value +0 dB 1→ PBO = Base Value +16 dB
12 bits 6 .. 2	Reserved		
12 bits 1.. 0	Loop ID	unsigned char	1 = Loop 1 2 = Loop 2

9.5.5.7.15 SHDSL Customer Side Performance Status - Message ID 141

This message provides the SHDSL Customer Side Performance Status. Device Fault shall be used to indicate hardware or software problems on the addressed unit. The definition of Device Fault is vendor dependent but is intended to indicate diagnostic or self-test results. DC Continuity Fault shall be used to indicate conditions that interfere with span powering such as short and open circuits. The definition of DC Continuity Fault is vendor dependent.

In octet 11, bits 7..4 are used to indicate that an overflow or reset has occurred in one or more of the modulo counters. Bits 7 and 5 shall indicate that an overflow has occurred since the last SHDSL Customer Side status response. For example, if more than 256 Errored Seconds occur between SHDSL Customer Side status responses, then the ES modulo counter will overflow. Bits 6 and 4 shall be used to indicate that one or more of the modulo counters have been reset for any reason (e.g. system powerup or a non-service-affecting reset). Bits 7 and 6 shall be cleared to 0 after a SHDSL Customer Side status response is sent to the STU-C. Bits 5 and 4 shall be cleared to 0 after a SHDSL Customer Side status response is sent to the STU-R.

TABLE 9 -19

SHDSL-Customer Side Performance Status Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 141	Message ID	
2 bit 7	Reserved		
bit 6	C - Power Backoff Status	bit	0 = default 1 = selected
bit 5	Device Fault	bit	0 = OK, 1 = Fault
bit 4	C - DC Continuity Fault	bit	0 = OK, 1 = Fault
bit 3	C - SNR Margin alarm	bit	0 = OK, 1 = alarm
bit 2	C - Loop Attenuation Alarm	bit	0 = OK, 1 = alarm
bit 1	C - SHDSL LOSW Failure Alarm	bit	0 = OK, 1 = alarm
bit 0	Reserved		set to 0
3	C - SHDSL SNR Margin (dB)	signed char (127 = NA)	
4	C - SHDSL Loop Attenuation (dB)	signed char (128 = NA)	
5	C - SHDSL ES Count modulo 256	unsigned char	
6	C - SHDSL SES Count modulo 256	unsigned char	
7-8	C - SHDSL CRC Anomaly Count modulo 65536	unsigned int	
9	C - SHDSL LOSW Defect Second Count modulo 256	unsigned char	
10	C - SHDSL UAS Count modulo 256	unsigned char	
11 bit 7	C - Counter Overflow Indication to STU-C		0 = OK 1 = Overflow
11 bit 6	C - Counter Reset Indication to STU-C		0 = OK 1 = Reset
11 bit 5	C - Counter Overflow Indication to STU-R		0 = OK 1 = Overflow
11 bit 4	C - Counter Reset Indication to STU-R		0 = OK 1 = Reset
11 bits 3 ..0	C-Power Back-Off Base Value (dB)	unsigned char	0 .. 15
12 bit 7	C-Power Back-Off Extension (dB)	bit	0→ PBO = Base Value +0 dB 1→ PBO = Base Value +16 dB
12 bits 6 .. 2	Reserved		
12 bits 1.. 0	Loop ID	unsigned char	1 = Loop 1 2 = Loop 2

9.5.5.7.16 Virtual Terminal Connect/Disconnect Request/Response (Msg. IDs 6, 7, 134)

Three messages are used to maintain (establish, tear down) virtual terminal sessions between units. A unit may request a connection but must wait for "connect" status response before using the connection. The connection shall remain until a disconnect request is processed or, if implemented, a timeout occurs. At least one session shall be supported by the STU-C. STU-R and SRU may silently ignore the connect request or may respond with a "no connect" status if terminal screens are not supported.

The connect/disconnect process is necessary for handling the case where keyboard messages are received from more than one device. If a unit cannot accommodate another connect request it shall send the "no connect" response.

The connect request message can be sent to cause a refresh of the current screen. When a connect request is accepted the "connect" response shall be transmitted, followed by screen messages with the current screen. If this is a new connection then the first screen shall be sent.

TABLE 9-20

Virtual Terminal Connect

Octet #	Contents	Data Type	Reference
1	Message ID 6 - Virtual Terminal Connect	Message ID	

TABLE 9-21

Virtual Terminal Disconnect

Octet #	Contents	Data Type	Reference
1	Message ID 7 - Virtual Terminal Disconnect	Message ID	

TABLE 9-22

Virtual Terminal Connect Response

Octet #	Contents	Data Type	Reference
1	Message ID 134 - Virtual Terminal Connect Response	Message ID	
2	Connection status		1 = connected 0 = no connect

9.5.5.7.17 Screen Message/Keyboard Message (MSG IDs 8, 136)

Keyboard and Screen messages are only sent over an active connection between units. Keyboard messages shall be 1 to 8 data octets per message. Queuing of keystrokes from the customer may affect user response times and should be done with care. Screen messages shall be 1 to 24 data octets per message, and their contents are vendor defined. See § 9.5.6 for more information on Screen/Keyboard messages.

TABLE 9-23

Keyboard Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 8 – Keyboard	Message ID	
Octet. 2 - L + 1	ASCII character(s) and escape sequences	char array	

TABLE 9-24

Screen Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 136 – Screen	Message ID	
Octet. 2 - L + 1	ASCII characters and escape sequences	char array	

9.5.5.7.18 Maintenance Request - System Loopback Messages (9)

The Maintenance Request-System Loopback Message contains loopback commands for all of the elements on the span. The contents of the Maintenance Request-System Loopback message are shown in Table 9-25. The System Loopback message shall have a broadcast destination address when sent from the STU-C. When optionally sent from the STU-R, the System Loopback message shall have the STU-C as its destination address. Upon reception of this message, each SRU and STU shall comply with its corresponding command field and respond to the sender with the Maintenance Status message. Note that the SRUs are numbered consecutively beginning with closest SRU to the STU-C. Each SRU shall determine its number by subtracting 2 from its network side EOC address. Since the network side EOC addresses must be known, the STU-R shall not use the System Loopback Message if the STU-C is offline. To invoke SRU loopbacks while the STU-C is offline, the STU-R shall use the Maintenance Request-Element Loopback message. (Maintenance request messages may also be used by the STU devices to poll for current loopback status, using the unchanged bit flags.)

TABLE 9-25

Maintenance Request - System Loopback Information Field

Octet #	Contents	Data Type	Reference
Octet 1	Message ID 9 – Maintenance Request-System Loopback		
Octet 2	STU-C Loopback Commands	Bit flags	Table 9-26
Octet 3	STU-R Loopback Commands	Bit flags	Table 9-26
Octet 4	SRU #1 Loopback Commands	Bit flags	Table 9-26
Octet 5	SRU #2 Loopback Commands	Bit flags	Table 9-26
Octet 6	SRU #3 Loopback Commands	Bit flags	Table 9-26
Octet 7	SRU #4 Loopback Commands	Bit flags	Table 9-26
Octet 8	SRU #5 Loopback Commands	Bit flags	Table 9-26
Octet 9	SRU #6 Loopback Commands	Bit flags	Table 9-26
Octet 10	SRU #7 Loopback Commands	Bit flags	Table 9-26
Octet 11	SRU #8 Loopback Commands	Bit flags	Table 9-26

TABLE 9-26

Loopback Command Bit Flag Definitions

Bit Positions	Definition
Bit 7	Reserved
Bit 6	Clear All Maintenance States (including any proprietary states)
Bit 5	Initiate Special Loopback
Bit 4	Terminate Special Loopback
Bit 3	Initiate Loopback toward the Network
Bit 2	Initiate Loopback toward the Customer
Bit 1	Terminate Loopback toward the Network
Bit 0	Terminate Loopback toward the Customer
NOTE - Bit set to 1 - perform action, Bit Set to 0 - no action taken, report current status.	

9.5.5.7.19 Maintenance Request - Element Loopback Message ID 10

The Maintenance Request-Element Loopback Message contains loopback commands for an individual element. The contents of the Maintenance Request-Element Loopback message are shown in Table 9-27. The Element Loopback message shall have an individual unit's destination address according to the data flow addresses described in § 9.5.2. Upon reception of the Element Loopback message, the addressed unit shall comply with the loopback commands and reply with the Maintenance Status Response message.

TABLE 9-27

Maintenance Request - Element Loopback Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 10 - Maintenance Request	Message ID	
2	Loopback Commands	Bit flags	Table 9-26

9.5.5.7.20 Maintenance Status Response Message ID 137

Maintenance status is sent in response to the Maintenance Request-System Loopback, Maintenance Request-Element Loopback, Status Request, and Full Status Request query messages. The "Special loopback" is defined for the STU-R as a Maintenance Termination Unit (MTU) loopback; it is not defined at other units.

TABLE 9-28

Maintenance Status Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 137 - Maintenance Status-Loopback	Message ID	
2 bit 7	Loopback Timeout Status	bit	0 = unchanged, 1 = changed
2 bit 6	Proprietary Maintenance State active	bit	0 = off, 1 = on
2 bit 5	Special loopback active	bit	0 = off, 1 = on
2 bit 4	Loopback active toward STU-R	bit	0 = off, 1 = on
2 bit 3	Loopback active toward STU-C	bit	0 = off, 1 = on
2 bit 2	Local or span-powered unit	bit	0 = span powered 1 = local powered
2 bit 1	Customer Tip/Ring Reversal	bit	0 = normal 1 = reversed
2 bit 0	Network Tip/Ring Reversal	bit	0 = normal 1 = reversed

9.5.5.7.21 Soft Restart/Power Backoff Disable Message ID 15

The purpose of this message is to switch a receiver between the default and selected modes of power backoff. If default mode is set, PBO shall be set to the default value. Otherwise, in selected mode, PBO may be negotiated through G.994.1 to another value. In order for a change in power backoff mode to take effect, the receiver must reactivate. The Soft Restart request shall cause the receiving unit to terminate the corresponding SHDSL connection and enter the Exception State (Figure 6-7). The connection shall not be terminated unless the corresponding Soft Restart bit is set in this message. The receiving unit shall wait 5 ± 1 s before terminating the SHDSL connection.

This message carries the command to set the power backoff mode. The power backoff mode received in this message shall be maintained as long as power is applied to the unit. Maintaining the power backoff mode in non-volatile storage is optional. Note that the configuration of power backoff mode applies to the receiver; i.e. the receiver requests a PSD mask based on both the received power and the configuration of its power backoff mode.

TABLE 9-29

Soft Restart Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 15 - Soft Restart/Backoff	Message ID	
2 Bits 7..2	Reserved		
2 Bit 1	Network Side Power Backoff Setting	bit	0 = default 1 = selected
2 Bit 0	Network Side Soft Restart (after 5 s)	bit	0 = no Restart 1 = Restart
3 Bits 7..2	Reserved		
3 Bit 1	Customer Side Power Backoff Setting	bit	0 = default 1 = selected
3 Bit 0	Customer Side Soft Restart (after 5 s)	bit	0 = no Restart 1 = Restart

9.5.5.7.22 Segment Management Message - (IDs 64-88, 192-216)

A range of Message IDs is reserved for segment management (e.g. continuous precoder update).

9.5.5.7.23 Proprietary Messages (IDs 112-119, 240-247)

A range of Message IDs is reserved for proprietary messages. It is the responsibility of the STU to address Proprietary Messages to the appropriate destination. An SRU shall either process or forward a proprietary message. A proprietary message shall not be broadcast.

9.5.5.7.24 Proprietary External Message (ID 120)

Support for external data ports is optional. No interface for an external data port is specified in this Recommendation. If an STU does not have an external data port then it shall ignore any received Proprietary External Messages.

TABLE 9-30

External Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 120 - External	Message ID	
2	Logical Port Number	Unsigned char	
octets 3.. N + 2	External message data (N octets)		

9.5.5.7.25 G.997.1 External Message (ID 121)

Support for G.997.1 [3] external messaging is optional. The interface for G.997.1 messages is beyond the scope of this Recommendation. If an STU does not have an interface for G.997.1 messaging, it shall ignore any received G.997.1 External Messages.

Logical port number FF_{16} is reserved for indicating the transport of SNMP packets, as described in § 6.3 of G.997.1. SNMP packets may be transmitted using one or more such messages.

TABLE 9-31

G.997.1 External Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 121	Message ID	
2	Logical Port Number	Unsigned char	
octets 3.. *N* + 2	G.997.1 External message data (*N* octets)		

9.5.5.7.26 Generic Unable to Comply (UTC) Message (ID 144)

The Generic UTC message should be sent back to the source unit in the event that the destination unit is unable to comply with the request. In this case, the definition of UTC is vendor dependent. Note that this message is not meant to replace the UTC bit in those response messages that contain a UTC bit.

TABLE 9-32

Generic Unable to Comply (UTC) Information Field

Octet #	Contents	Data Type	Reference
1	Message ID 144 – Generic UTC	Message ID	
2	Message ID of request message	Unsigned char	

9.5.6 Examples of Virtual Terminal Control Functions.

This informative note gives examples of some common ANSI X3.4-1986 (R1997) [B3] escape sequences.

TABLE 9-33

Examples of ANSI X3.4-1986 (R1997) Control Functions

Description	Format	Comments
Erase entire screen (ED)	ESC [2 J	
Position cursor (CUP)	ESC [RR;CCH	See NOTE
Position cursor (in column 1)	ESC [RRH	subset of Position cursor
Home cursor	ESC [H	subset of Position cursor

NOTE - ESC has the value of $1B_{16}$. RR is the row number; CC is the column number expressed as ASCII digits. As an example, row 4 column 12 would encode as ESC [4;12H. The hexadecimal equivalent of this sequence is $1B_{16}$ $5B_{16}$ 34_{16} $3B_{16}$ 31_{16} 32_{16} 48_{16}. The screen starts with row 1, column 1.

10 Clock Architecture

10.1 Reference Clock Architecture

Due to the multiple applications and variable bit rates called for in SHDSL, a flexible clocking architecture is required. The STU-C and STU-R symbol clocks are described in terms of their allowed synchronization references.

The SHDSL reference configuration permits the flexibility to provide a symbol clock reference based on the sources shown in Figure 10-1. It illustrates the clock reference options in the context of a simplified SHDSL reference model. Table 10-1 lists the normative synchronization configurations as well as example applications.

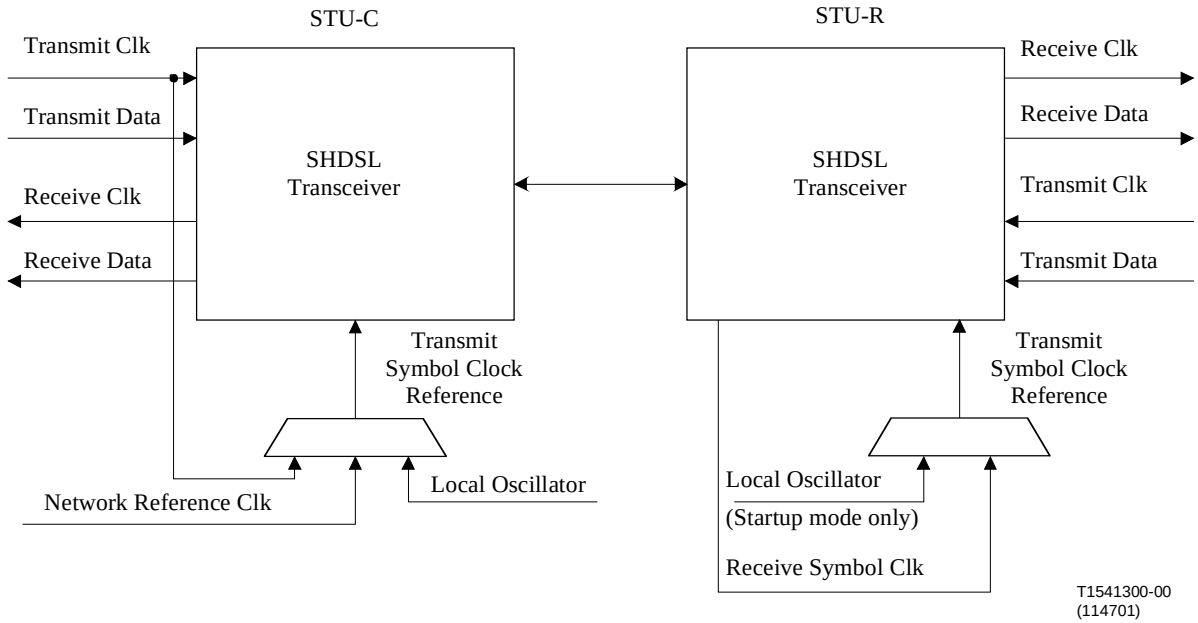


FIGURE 10-1

Reference Clock Architecture

TABLE 10-1

Clock Synchronization Configurations

Mode Number	STU-C Symbol Clock Reference	STU-R Symbol Clock Reference	Example Application	Mode
1	Local oscillator	Received symbol clock	"Classic" HDSL.	Plesiochronous
2	Network reference clock	Received symbol clock	"Classic" HDSL with embedded timing reference.	Plesiochronous with timing reference
3a	Transmit data clock or network reference clock	Received symbol clock	Main application is synchronous transport in both directions.	Synchronous
3b	Transmit data clock	Received symbol clock	Synchronous downstream transport and bit-stuffed upstream is possible.	Hybrid: downstream: synchronous upstream: plesiochronous

10.2 Clock Accuracy

At all rates, the transmit symbol clock during data mode from any SHDSL device shall be accurate to within ±32 ppm of the nominal frequency. During activation, the STU-C shall maintain ±32 ppm accuracy of its transmit symbol clock, but the STU-R transmit symbol clock may vary up to ±100 ppm.

10.3 Definitions of Clock Sources

The following definitions shall apply to the clock sources shown in Figure 10-1.

10.3.1 Transmit symbol clock reference

A reference clock from which the actual transmit symbol clock is derived (i.e. the STU's transmit symbol clock is synchronized to this reference).

10.3.2 Local oscillator

A clock derived from an independent local crystal oscillator.

10.3.3 Network reference clock

A primary reference clock derived from the network.

10.3.4 Transmit data clock

A clock that is synchronous with the transmitted data at the application interface.

10.3.5 Receive symbol clock

A clock that is synchronous with the downstream received symbols at the SHDSL line interface. This clock is used as the transmit symbol clock reference in the STU-R.

10.3.6 Receive Clock

A clock that is synchronous with the received data at the application interface.

10.4 Synchronization to Clock Sources

In synchronous mode, the STU-C can be synchronized to the transmit data clock or to a network reference clock. If a network reference clock is used, the transmit data clock must be synchronized to the network reference clock. (The various transmit data rates are independent of the reference clock frequency).

When available, the network reference clock shall be either a fundamental 8 kHz network clock or a related reference clock at some multiple of 8 kHz. Such reference clocks are typically 1 544 MHz or 2 048 MHz, although in some applications other frequencies, such as 64 kHz, may be available. These related clocks include implicit 8 kHz[2] timing signals. Selection of a specific network clock reference frequency shall be application dependent.

11 Electrical Characteristics

This section specifies conformance tests for SHDSL equipment. These out-of-service tests verify the electrical characteristics of SHDSL metallic interfaces.

11.1 Longitudinal Balance

Longitudinal balance or longitudinal conversion loss (LCL) is a figure of merit describing the coupling between longitudinal V_L (common mode) and metallic V_M (normal mode) signal components. This term is equivalent to the familiar common mode rejection ratio (CMRR) and defined as follows:

$$\text{Longitudinal Balance (dB)} = 20\log\left|\frac{V_L}{V_M}\right|$$

Longitudinal balance at the SHDSL loop interface shall be measured with a coupling circuit having a metallic termination of 135 Ω and a longitudinal termination of 33.8 Ω (Figure 11-1). Example coupling circuits are shown in Appendix I. This test shall be performed with the DUT transmitter turned off (quiet mode) and with span power circuitry (in either CO and RT units) activated by an appropriate external DC current source/sink. The active power feed requirement may be waived for locally powered systems.

---

[2] The 6 ms SHDSL frame for synchronous data transport and the network 8 kHz clock have a fixed relationship. Each SHDSL frame contains 48(1 + i + n × 8) bits (i = 0 ..7 and n = 3 .. 36). The relationship can be calculated with: T = 6 ms/48 = 125 µs and f = 1/T = 8 kHz. At the STU-R, an 8 kHz clock signal can be derived from the synchronous 6 ms frame.

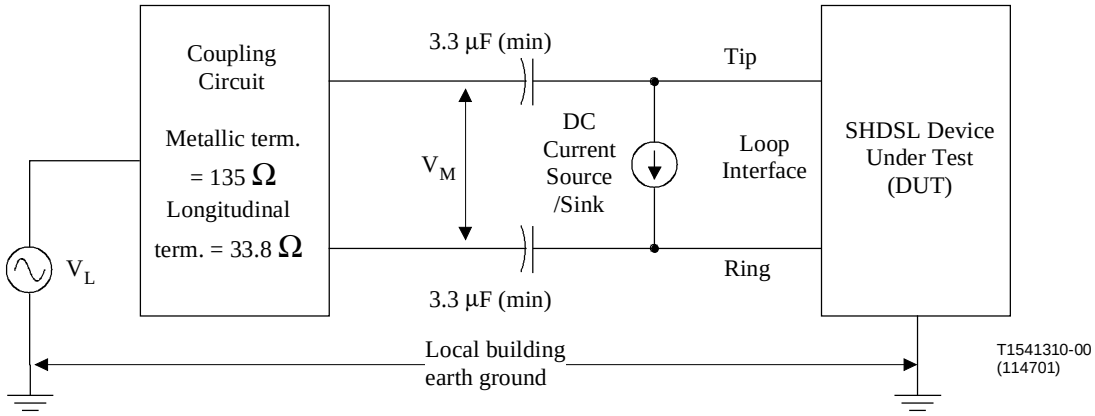


FIGURE 11-1

Longitudinal Balance Measurement

The measured longitudinal balance at the SHDSL loop interface shall lie above the specified limit mask defined in Figure 11-2. The values of the parameters in the figure are region-specific and are specified in § A.5.4 and § B.5.4. The longitudinal test circuit shall be calibrated such that when a 135 Ω resistor (placed across tip and ring) is substituted for the device under test and the DC current source/sink is disconnected, the measured longitudinal balance shall be at least 20 dB above the limit mask. The longitudinal balance shall be measured over the frequency range of 20 kHz to 2 MHz.

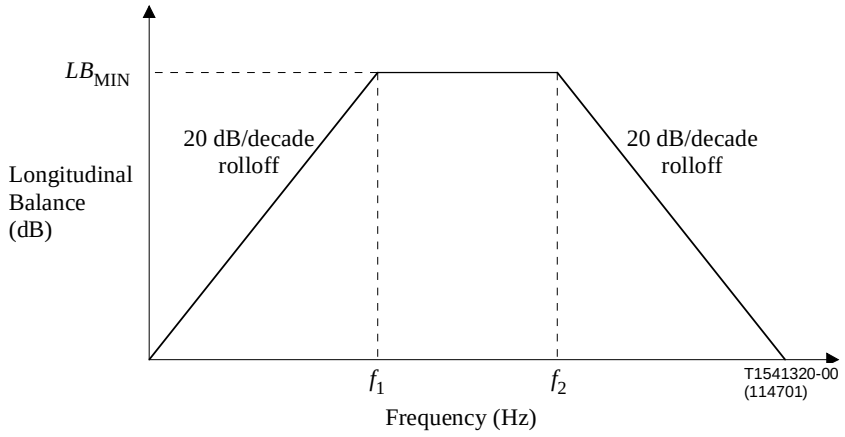


FIGURE 11-2

Longitudinal Balance Limit Mask

11.2 Longitudinal Output Voltage

Longitudinal output voltage at the SHDSL loop interface shall be measured with a coupling circuit having a metallic termination of 135 Ω and a longitudinal termination of 33.8 Ω as shown in

Figure 11-3. Example coupling circuits are shown in Appendix I. This test shall be performed with the transmitter active (sending random data) and the span power circuitry (in either CO and RT units) activated by an appropriate external DC current source/sink. The active power feed requirement may be waived for locally powered systems.

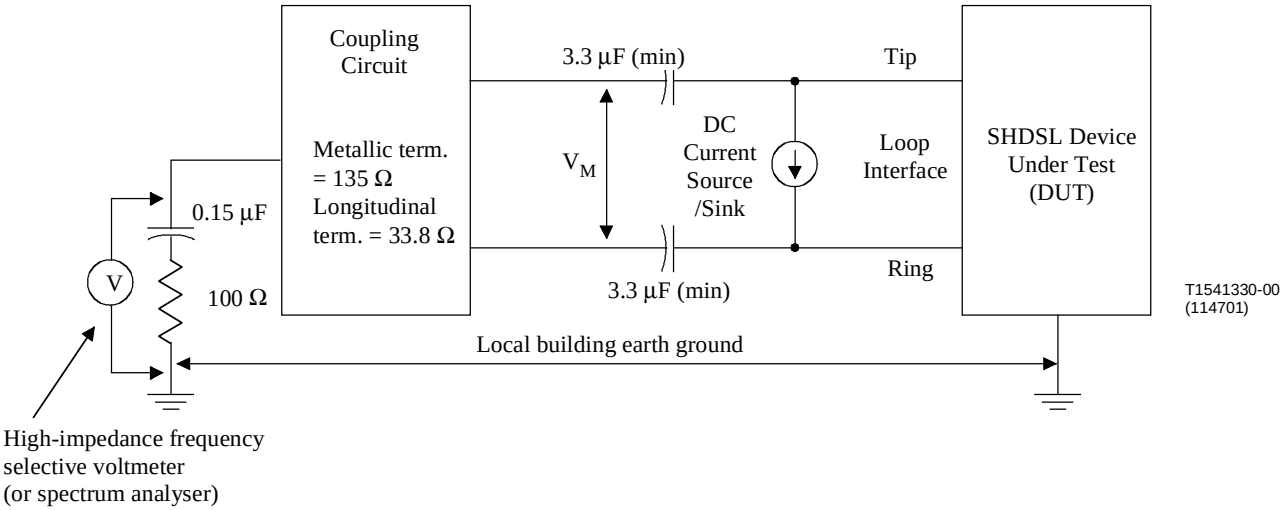


FIGURE 11-3

Longitudinal Output Voltage Measurement

The measured longitudinal output rms voltage at the SHDSL loop interface shall be less than –50 dBV over any 4 kHz frequency band when averaged over one second periods. The measurement frequency range is region-specific and is specified in § A.5.5 and § B.5.5.

11.3 Return Loss

This test measures return loss at the SHDSL loop interface with respect to a 135 Ω reference (line) impedance. In SHDSL applications, return loss is generally used as a measure of termination impedance distortion (deviation in both magnitude and phase from the reference impedance value). Return loss limits are necessary to prevent large termination mismatches between equipment from compliant vendors. Return loss may be measured directly using an impedance analyser or indirectly as a voltage output in a bridge circuit. For either method care must be taken to prevent measurement errors from possible unintentional circuit paths between the common ground of the measuring instrument(s) and the DUT power feed circuitry. In addition, when measuring under span powered conditions, the test instrument must be galvanically isolated from the loop interface to prevent damaging the test equipment with the high voltage DC power feed. For measurements performed with an impedance analyser return loss is defined as follows:

$$\text{Return Loss}(f) = 20\log\left|\frac{Z_{TEST}(f) + Z_{REF}}{Z_{TEST}(f) - Z_{REF}}\right|$$

where $Z_{TEST}(f)$ = measured complex impedance at frequency f at the DUT loop interface and

Z_{REF} = reference impedance (135 Ω).

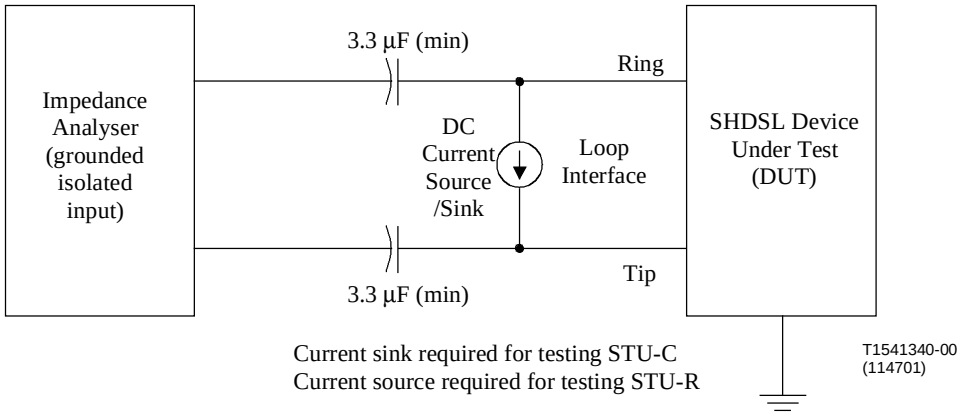


FIGURE 11-4

Return Loss Impedance Analyser Test Method

For measurements performed with a test bridge the return loss is defined as follows:

$$\text{Return Loss}(f) = 20\log\left|\frac{V_{IN}(f)}{V_{OUT}(f)}\right|$$

An example return loss test bridge is shown in Appendix I.

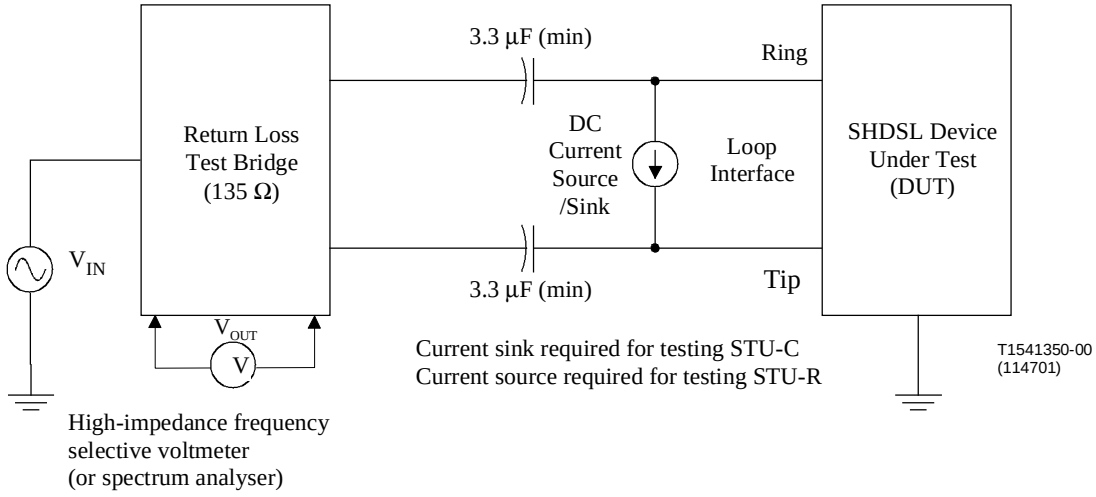


FIGURE 11-5

Return Loss Bridge Test Method

The return loss test shall be performed with the DUT transmitter turned off (quiet mode). The DUT may be tested span powered or locally powered as required by the intended application of the DUT. For span powered applications, if the DUT is an STU-C the test shall be performed with the span power supply activated and an appropriate DC current sink (with high AC impedance) attached to the test circuit. If the DUT is an STU-R the test shall be performed with power (DC voltage)

applied at the loop interface (TIP/RING) by an external voltage source feeding through an AC blocking impedance. Note that the DC current source/sink must present a high impedance (at signal frequencies) to common ground.

The nominal driving point impedance of the SHDSL loop interface shall be 135 Ω. Return loss shall be measured with either the impedance analyser method of Figure 11-4 or the bridge method of Figure 11-5. The measured return loss values relative to 135 Ω shall lie above the limit mask specified in Figure 11-6. The values of the parameters are region-specific, and are specified in § A.5.2 and § B.5.2. The loop interface return loss shall be measured over the frequency range of 1 kHz to 2 MHz.

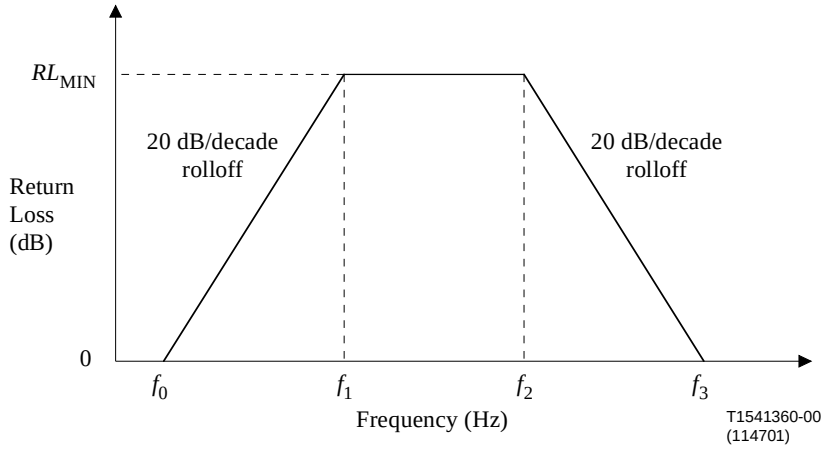


FIGURE 11-6

Return Loss Limit Mask

11.4 Transmit Power Testing

The total average transmit power may be tested while span powered or locally powered as required by the intended application of the DUT. For span powered applications, if the DUT is an STU-C the test shall be performed with the span power supply activated and an appropriate DC current sink (with high AC impedance) attached to the test circuit. If the DUT is an STU-R the test shall be performed with power (DC voltage) applied at the loop interface (TIP/RING) by an external voltage source feeding through an AC blocking impedance. The test circuit must contain provisions for DC power feed and possibly transformer isolation for the measurement instrumentation. Note that the DC current source/sink must present a high impedance (at signal frequencies) to common ground.

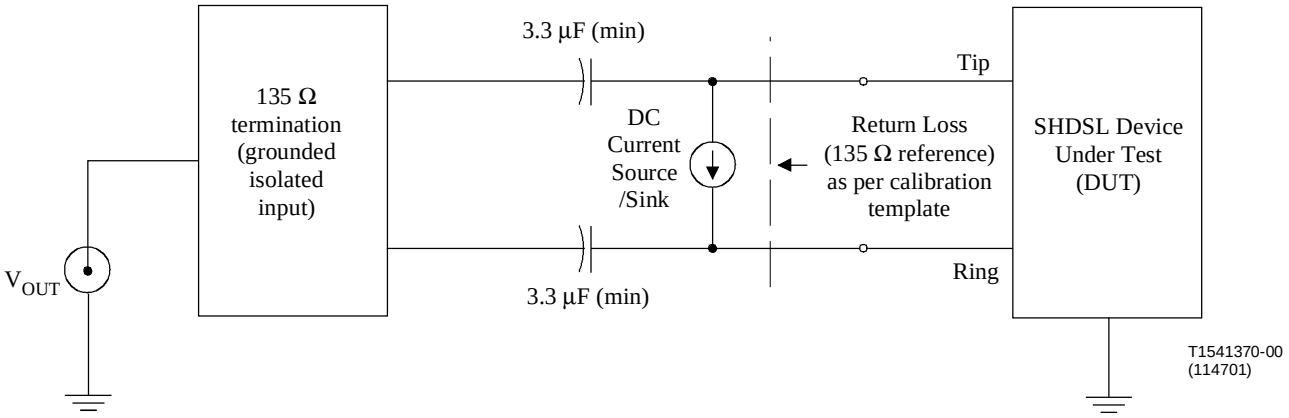


FIGURE 11-7

PSD/Total Power Measurement Setup

11.4.1 Test Circuit

The test circuit must contain provisions for DC power feed and possibly transformer isolation for the measurement instrumentation. Transformer isolation of the instrumentation input prevents measurement errors from unintentional circuit paths through the common ground of the instrumentation and the DUT power feed circuitry. When the driving point impedance of the test circuit meets the calibration requirements defined in § 11.4.2 the test circuit will not introduce more than ± 0.25 dB error with respect to a perfect 135 Ω test load. An example test circuit is shown in Appendix I. Note that the same circuit may be used for measuring total transmit power and transmit PSD.

11.4.2 Test Circuit Calibration

The nominal driving point impedance of the test circuit shall be 135 Ω. The minimum return loss with respect to 135 Ω over the frequency band of 1 kHz to 3 MHz shall be 35 dB from 10 kHz to 500 kHz with a slope of 20 dB/decade below and above these corner frequencies.

NOTE - 35 dB return loss will allow ±0.20 dB measurement error with respect to the nominal 135 Ω value.

11.4.3 Total Transmit Power Requirement

The average transmit power of the STU-C shall be measured while continuously sending signal S_c (§ 6.2.2.2) with the appropriate transmit PSD, as specified in § A.3.3.8 or § B.4. The average transmit power of the STU-R shall be measured while continuously sending signal S_r (§ 6.2.2.3) with the appropriate transmit PSD, as specified in § A.3.3.8 or § B.4. The measured total power shall meet the applicable § A.3.3.8 or § B.4 requirements. This power measurement in activation mode will be 0.2 dB lower than the associated data mode transmit power due to the 2-PAM constellation definition.

11.4.3.1 Transmit Power Spectral Density Test Procedure

The transmit power spectral density (PSD) may be tested span powered or locally powered as required by the intended application of the DUT. For span powered applications, if the DUT is an STU-C the test shall be performed with the span power supply activated and an appropriate DC

current sink (with high AC impedance) attached to the test circuit. If the DUT is an STU-R the test shall be performed with power (DC voltage) applied at the loop interface (TIP/RING) by an external voltage source feeding through an AC blocking impedance.

The transmit power spectral density for the STU-C and STU-R shall be measured with signals as defined in § 11.4.3. The transmit power spectral density shall be measured over the frequency range of 1 kHz to 3 MHz. The STU-C transmit signal shall be compliant with the appropriate § A.3.3.8 or § B.4 PSD requirements. The STU-R transmit signal shall be compliant with the appropriate § A.3.3.8 or § B.4 PSD requirements.

11.4.3.2 PSD Test Circuit and Calibration

The test circuit must contain provisions for DC power feed and possibly transformer isolation for the measurement instrumentation. Transformer isolation of the instrumentation input prevents measurement errors from unintentional circuit paths through the common ground of the instrumentation and the DUT power feed circuitry. The test circuit shall meet the requirements of § 11.4.2.

11.5 Signal Transfer Delay

The STU shall be capable of providing PMD-layer one-way, single-span latency of 500 μs or less for user data rates of 1.5 Mbit/s and above, and 1.25 ms or less for user data rates below 1.5 Mbit/s as measured between the α and β interfaces.

12 Conformance Testing

12.1 Micro-Interruptions

A micro-interruption is a temporary interruption due to external mechanical action on the copper wires constituting the transmission segment, for example, at a cable splice. Splices can be hand made wire-to-wire junctions, and during cable life oxidation phenomena and mechanical vibrations can induce micro-interruptions at these critical points. Example causes of this impairment include a large motor vehicle driving over a buried cable installation or an aerial cable movement from wind forces.

The effect of a micro-interruption on the transmission system can be a failure of the digital transmission link, together with a failure of the span power feeding (if provided) for the duration of the micro-interruption. The operating objective is that in the presence of a micro-interruption of specified maximum length the system shall not reset, and the system shall automatically reactivate with a complete start-up procedure if a reset occurs due to an interruption.

The configuration for micro-interruption susceptibility testing is shown in Figure 12-1. In this arrangement a periodic trigger signal *S* stimulates a normally closed micro-relay device inducing periodic micro-interruptions on the transmission link. Note that the micro-interruptions are induced on one termination at a time. The test loops shall be composed of 1.5 km of 0.4 mm (or 5 000' of 26 AWG) copper wire, and the tests shall be conducted at the maximum supported data rate. Using the test arrangement as described in Figure 12-1 with local powering on, the SHDSL transceivers shall not be reset by a micro-interruption of at least t = 10 ms when stimulated with a signal of period T = 5 s for a test interval of 60 s at a single termination. The micro-interruptions shall be induced at both the STU-C and STU-R terminations. This test shall be repeated with span-powering on and a micro-interruption of at least t = 1 ms.

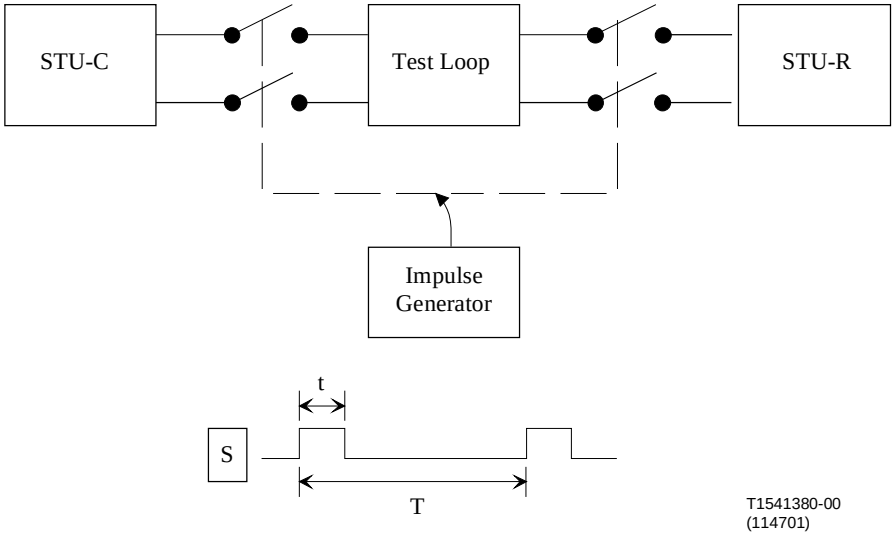


FIGURE 12-1

Micro-Interruption Test Circuit

ANNEX A

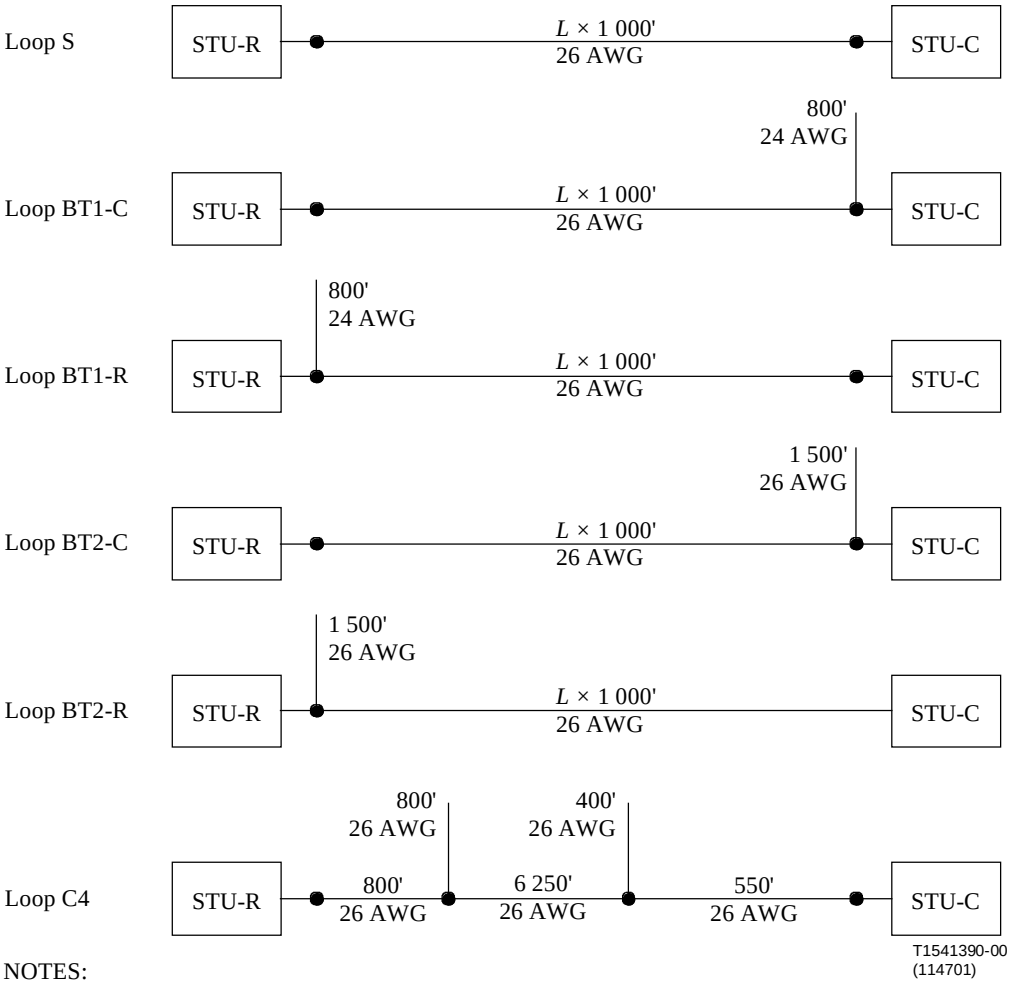
Regional Requirements - Region 1

A.1 Scope

This annex describes those specifications that are unique to SHDSL systems operating under conditions such as those typically encountered within the North American network. The clauses in this annex provide the additions and modifications to the corresponding clauses in the main body.

A.2 Test Loops

The primary constants for the following test loops are listed in Annex A of ITU-T G.996.1 [6]. Note that the test loops shown in Figure A-1 are PIC and specified at 70° F (21.1º C). Loop 0 is the null loop: ≤ 10' and ≤ 26 AWG.



NOTES:
AWG = American Wire Gauge; 26 AWG = 0.4 mm, 24 AWG = 0.5 mm
Distances in feet ('): 1 000' = 0.3048 km

FIGURE A-1

Test Loops

A.3 Performance Tests

This section specifies performance tests for SHDSL equipment. These out-of-service tests verify the performance of SHDSL in impaired environments.

Figure A-2 shows the test setup for measuring the performance of SHDSL systems in the presence of noise impairments. The test system consists of an SHDSL central office transceiver (STU-C) and a remote end transceiver (STU-R). The SHDSL transceivers are connected by a test loop. Simulated noise is locally injected into the test loop through the specified coupling circuit at the receiving transceiver.

Bit-error ratio (BER) measurement is performed by applying a pseudo-random binary sequence (PRBS) test signal at one transceiver input and detecting errors in the received PRBS data stream of the other transceiver. The PRBS signal shall have a minimum period of 2^{23} - 1. BER measurement shall be performed for both directions of transmission and the tests in each direction shall be performed in full-duplex mode with both SHDSL transceivers simultaneously transmitting data. In all cases these noise impairment tests shall be performed one unit at a time (i.e. the STU-C and STU-R are not impaired simultaneously) and with noise from only one impairment source active at a time.

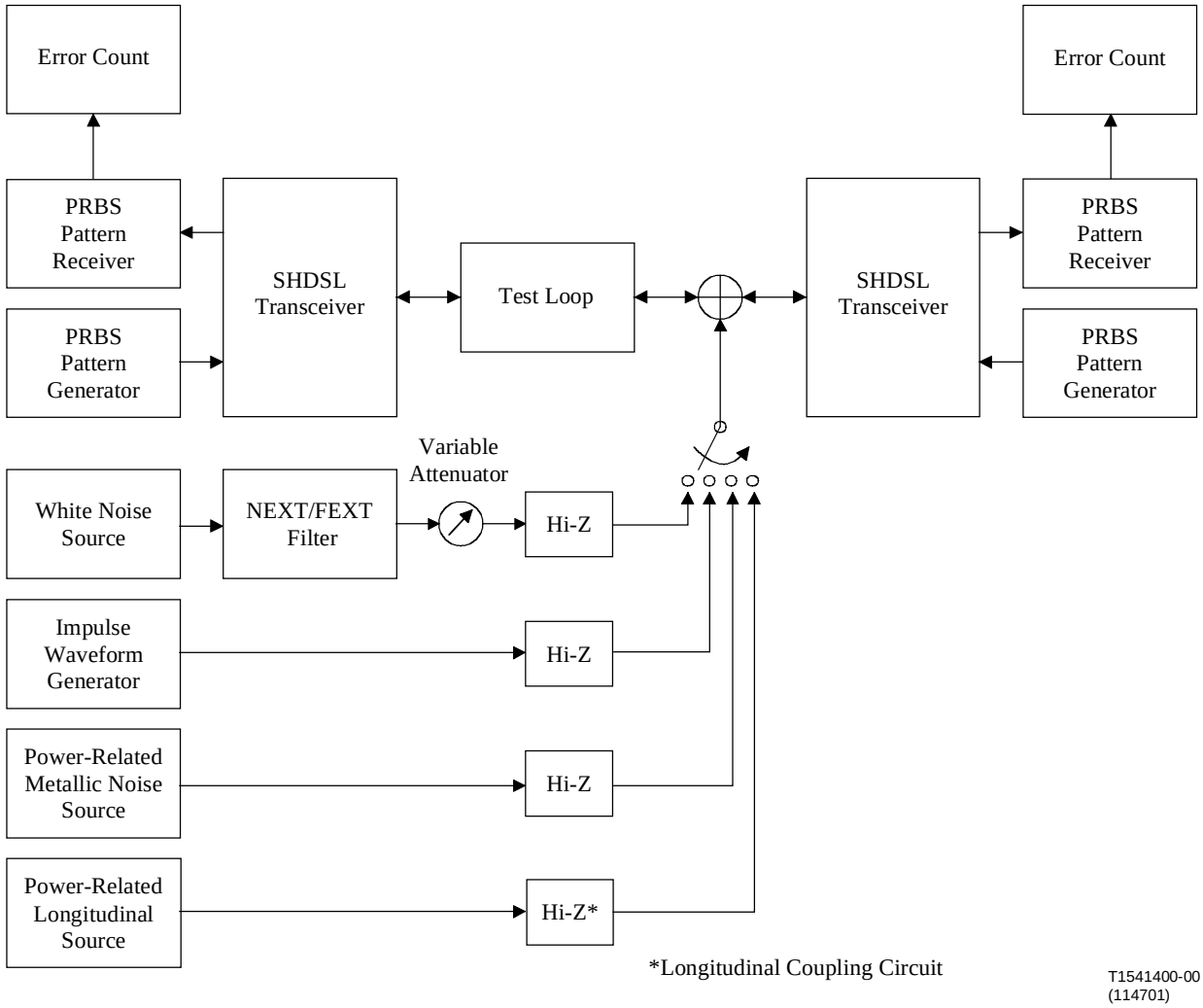


FIGURE A-2

Crosstalk Margin and Impulse Noise Test Setup

A.3.1 Crosstalk Margin Tests

A.3.1.1 Crosstalk Noise Injection

Simulated crosstalk (NEXT and FEXT) is introduced by injecting a calibrated, filtered Gaussian noise source into the test circuit. The crosstalk shall be locally injected into the test loop at the receiving transceiver through a balanced high-impedance parallel-connected feed network. The high-impedance parallel-connected feed network allows injection of the desired crosstalk power level without disturbing the transmission characteristics or driving point impedance of the test loop. The injection circuit shall have a Thevenin output impedance of at least 4 kΩ. An example crosstalk signal injection circuit is shown in Figure I-1.

A.3.1.2 Calibration Accuracy of Crosstalk Generator

The simulated crosstalk shall have the total power and the power spectral density (PSD) defined in § A.3.3. However, if the method of generating simulated crosstalk is as defined in Figure A-2, then the power level and PSD accuracy will depend on the accuracy of the filters designed to shape the

white noise for each injected crosstalk source. The highest level of accuracy is required within the frequency band (or bands) corresponding to the largest values of the PSD for each crosstalk source.

For each specified crosstalk source, the accuracy of the simulated PSD obtained shall be ±1.0 dB within the ideal PSD template (defined by the equations in § A.3.3) over the frequency band(s) where the ideal PSD template is within 30 dB of its maximum value. The measured average power (integral of the crosstalk PSD function) for each specified crosstalk source shall be within ±0.25 dB of the integrated power of the ideal specified crosstalk PSD template (§ A.3.3).

The white noise source of Figure A-2 shall cover the frequency band from DC to 1.5 MHz and have a Gaussian amplitude distribution with a crest factor of at least 5.0.

A.3.1.3 Calibration Measurement of Crosstalk Generator

The PSD and average power for each crosstalk test scenario shall be calibrated by measuring the output of the crosstalk injection circuit with the test loop replaced by a load of two parallel 135 Ω resistors (67.5 Ω) and no connected terminal equipment. The two parallel 135 Ω resistors simulate the terminating load of a zero-length loop. The crosstalk signal shall be measured as a voltage by a high-impedance frequency-selective voltmeter (i.e. spectrum analyser) and converted into a power level assuming a 135 Ω reference impedance. This procedure effectively measures the crosstalk power fed into a single resistor (one side of the loop only). The measured crosstalk PSD(s) and average crosstalk power(s) coupled into the calibration load must remain within the limits defined in § A.3.1.2 for each specified crosstalk scenario defined in § A.3.1.6.

A.3.1.4 Calibration of Loop Simulator

There is significant variation in loop insertion loss for the same loop model on loop simulators from both different and identical manufacturers. Typical loop simulators may exhibit insertion loss variations greater than ±1.0 dB of the ideal loop model over the SHDSL signal band. Insertion loss variation of loop simulators may cause significant variation of measured system noise margin. To minimize measurement variation caused by the loop simulator, the crosstalk generator output power may be adjusted to maintain a consistent SNR at the receiver input. The calibration procedure is as follows:

1) Given the discrete form of the DFE-based SNR formula, SNR_{dB}, given below

$$SNR_{dB} = \frac{1}{M}\sum_{k=1}^{M} 10\log_{10}\left(\begin{array}{l} 1+\dfrac{S(f_{sym}-f_k)\left|H(f_{sym}-f_k)\right|^2}{N(f_{sym}-f_k)}+\dfrac{S(f_k)\left|H(f_k)\right|^2}{N(f_k)}+ \\ \dfrac{S(2f_{sym}-f_k)\left|H(2f_{sym}-f_k)\right|^2}{N(2f_{sym}-f_k)}+\dfrac{S(f_{sym}+f_k)\left|H(f_{sym}+f_k)\right|^2}{N(f_{sym}+f_k)} \end{array}\right)$$

calculate *SNR1*, the ideal receive signal-to-noise ratio, by setting *SNR1* equal to SNR_{dB} where *S(f)* shall be the nominal far-end transmit signal power spectral density (*NominalPSD(f)* from § A.4), $|H(f)|^2$ shall be the magnitude squared of the ideal loop insertion gain function, *N(f)* shall be the injected crosstalk noise power spectral density ($PSD_{Case\text{-}n}(f)$ from § A.3.3.9), and f_{sym} shall be the transmit symbol rate. For this application use $f_k = k \times 1000$, k =1…M, where M is the maximum value of k such that $M \times 1000 < f_{sym} \leq (M+1) \times 1000$. The ideal loop insertion gain function shall be calculated from the primary constants of twisted pair copper as defined in Annex A of ITU-T G.996.1 [6].

2) Measure the insertion loss of the loop simulator with 135 Ω terminations at points f_k defined in Step 1. Note that the termination return loss with respect to 135 Ω should be greater than

35 dB from 20 kHz to f_{sym}. to ensure insertion loss measurement accuracy within 0.25 dB over the main part of the SHDSL signal band. An example insertion loss measurement setup is shown in Figure A-3. The measured loss in dB of the loop at each frequency shall be within 5% (in dB) of the theoretical loop insertion loss function as calculated in Step 1. As the measurements for the calibration procedure are easily made with error, the return loss measurement set used to verify the 35 dB return loss of the test fixture terminations shall be calibrated with a known return loss test load of at least 55 dB over the range of 20 kHz to 500 kHz. In addition, the line simulator should exhibit a longitudinal balance of 35 dB or better for frequencies in the range of 0 to f_{sym}.

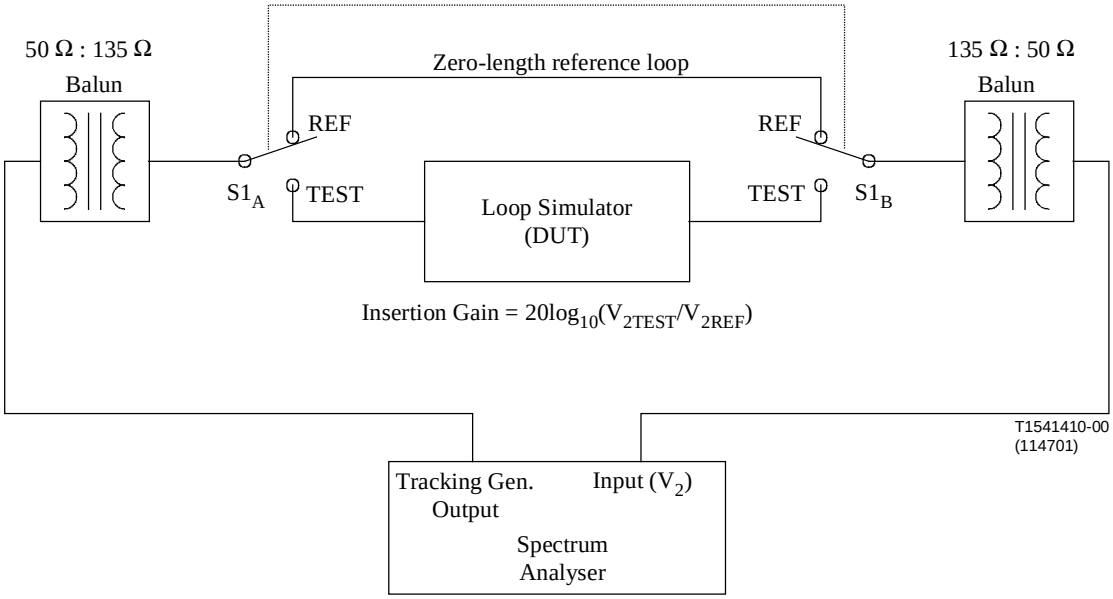


FIGURE A-3

Example Loop Insertion Loss Measurement Setup

3) Calculate SNR2, the measured receive signal-to-noise ratio, by setting *SNR2* equal to SNR_{dB} from step 1 where $|H(f)|^2$ shall be the magnitude squared of the measured loop insertion gain function from step 2 above, and *S(f)*, *N(f)*, f_{sym}, and f_k shall be the same as in step 1 above.

4) Adjust the noise margin target in Table A-1 by Δ = (SNR2 – SNR1) dB. Note that a negative difference corresponds to a decrease in crosstalk generator power. Note that this procedure assumes the crosstalk generator was previously calibrated as per sections § A.3.1.2 and § A.3.1.3. All crosstalk power adjustments shall be limited to 3.0 dB maximum. Test setups requiring greater than 3.0 dB crosstalk power adjustment shall not be valid.

A.3.1.5 Crosstalk Margin Compliance Procedure

The SHDSL transceivers shall have noise margins that meet or exceed the values listed in Table A-1 for the specified test loop and crosstalk combinations. The definitions of the test loops are given in Figure A-1, and specifications for the crosstalk PSDs are given in § A.3.3. The test for noise margin compliance shall be defined as follows:

1) Calibrate the crosstalk injection circuit (using the calibration load of 67.5 Ω) to the corresponding PSD and total power value specified in § A.3.3.

2) Increase the injected crosstalk power by the corresponding noise margin value specified in Table A-1.

3) Using the test setup from Figure A-2, activate the SHDSL transceivers and allow a minimum 5 minute fine-tuning period.

4) Measure the BER over a minimum of 10^9 bits.

5) The measured BER at each end shall be less than 10^{-7}.

A.3.1.6 Crosstalk Interference Requirements

Table A-1 shows the minimum set of test loops and crosstalk combinations required for testing SHDSL margins. A compliant unit shall pass the BER test described in § A.3.1.5 for all crosstalk scenarios and test loops defined in Table A-1. 0 dB Power Backoff shall be used for both the STU-C and STU-R.

TABLE A-1

Crosstalk Scenarios & Required SHDSL Noise Margins[3]

Test	Test Loop (from Figure A-1)	*L* (×1 000')	Test Unit	Payload Data Rate (kbps)	PSD	Interferer Combination	Required Margin (dB)
1	C4	-	STU-C	1 544	asymmetric	24T1 + 24 SHDSL	$5 + \Delta^*$
2	C4	-	STU-C	1 544	asymmetric	39 SHDSL	$5 + \Delta^*$
3	C4	-	STU-C	1 544	asymmetric	24 FDD ADSL + 24 HDSL	$5 + \Delta^*$
4	S	9.0	STU-C	1 544	asymmetric	24T1 + 24 SHDSL	$5 + \Delta^*$
5	S	9.0	STU-C	1 544	asymmetric	39 SHDSL	$5 + \Delta^*$
6	S	9.0	STU-C	1 544	asymmetric	24 FDD ADSL + 24 HDSL	$5 + \Delta^*$
7	C4	-	STU-R	1 544	asymmetric	24T1 + 24 SHDSL	$5 + \Delta^*$
8	S	9.0	STU-R	1 544	asymmetric	24T1 + 24 SHDSL	$5 + \Delta^*$
9	S	6.3	STU-C	2 304	symmetric	24-T1 + 24 SHDSL asym 1 544	$5 + \Delta^*$
10	BT1-C	5.2	STU-C	2 304	symmetric	24-T1 + 24 SHDSL asym 1 544	$5 + \Delta^*$
11	BT1-C	5.2	STU-C	2 304	symmetric	49-SHDSL	$5 + \Delta^*$
12	S	6.3	STU-R	2 304	symmetric	49-SHDSL	$5 + \Delta^*$
13	BT1-R	5.2	STU-R	2 304	symmetric	49-SHDSL	$5 + \Delta^*$
14	BT1-R	5.2	STU-R	2 304	symmetric	24-T1 + 24 SHDSL asym 1 544	$5 + \Delta^*$
15	S	6.8	STU-C	2 048	symmetric	24-SHDSL + 24-FDD ADSL	$5 + \Delta^*$
16	BT1-C	5.6	STU-C	2 048	symmetric	49-SHDSL	$5 + \Delta^*$
17	BT1-C	5.6	STU-C	2 048	symmetric	24-T1 + 24 SHDSL asym 1 544	$5 + \Delta^*$
18	S	6.8	STU-R	2 048	symmetric	49-SHDSL	$5 + \Delta^*$
19	BT1-R	5.6	STU-R	2 048	symmetric	49-SHDSL	$5 + \Delta^*$
20	BT1-R	5.6	STU-R	2 048	symmetric	24-T1 + 24 SHDSL asym 1 544	$5 + \Delta^*$
21	S	7.9	STU-C	1 544	symmetric	39-SHDSL asym 1 544	$5 + \Delta^*$
22	BT1-C	6.4	STU-C	1 544	symmetric	24-FDD ADSL + 24 SHDSL asym 1 544	$5 + \Delta^*$
23	BT1-C	6.4	STU-C	1 544	symmetric	24-SHDSL + 24-FDD ADSL	$5 + \Delta^*$
24	S	7.9	STU-R	1 544	symmetric	49-SHDSL	$5 + \Delta^*$
25	BT1-R	6.4	STU-R	1 544	symmetric	24-T1 + 24 SHDSL asym 1 544	$5 + \Delta^*$
26	BT1-R	6.4	STU-R	1 544	symmetric	49-SHDSL	$5 + \Delta^*$
27	S	11.0	STU-C	768	symmetric	49-HDSL	$5 + \Delta^*$
28	BT1-C	10.2	STU-C	768	symmetric	49-SHDSL	$5 + \Delta^*$

[3] The crosstalk scenarios listed in this table were developed under the assumption of a 50 pair cable binder. Cablebinders of other sizes are for further study.

29	BT1-C	10.2	STU-C	768	symmetric	49-HDSL	5 + Δ*
30	S	11.0	STU-R	768	symmetric	49-HDSL	5 + Δ*
31	BT1-R	10.2	STU-R	768	symmetric	49-SHDSL	5 + Δ*
32	BT1-R	10.2	STU-R	768	symmetric	49-HDSL	5 + Δ*
33	S	11.2	STU-C	768	asymmetric	49-HDSL	5 + Δ*
34	BT1-C	10.4	STU-C	768	asymmetric	49-HDSL	5 + Δ*
35	BT1-C	10.4	STU-C	768	asymmetric	24-FDD ADSL + 24-HDSL	5 + Δ*
36	S	11.2	STU-R	768	asymmetric	24-T1 + 24 HDSL	5 + Δ*
37	BT1-R	10.4	STU-R	768	asymmetric	24-T1 + 24-SHDSL	5 + Δ*
38	BT1-R	10.4	STU-R	768	asymmetric	39-FDD ADSL	5 + Δ*
39	S	14.8	STU-C	384	symmetric	24-SHDSL + 24-DSL	5 + Δ*
40	BT2-C	13.8	STU-C	384	symmetric	24-SHDSL + 24-DSL	5 + Δ*
41	BT2-C	13.8	STU-C	384	symmetric	49-SHDSL	5 + Δ*
42	S	14.8	STU-R	384	symmetric	24-SHDSL + 24-DSL	5 + Δ*
43	BT2-R	13.8	STU-R	384	symmetric	24-SHDSL + 24-DSL	5 + Δ*
44	BT2-R	13.8	STU-R	384	symmetric	49-SHDSL	5 + Δ*
45	S	17.2	STU-C	256	symmetric	49-DSL	5 + Δ*
46	BT2-C	16.4	STU-C	256	symmetric	49-DSL	5 + Δ*
47	BT2-C	16.4	STU-C	256	symmetric	24-SHDSL + 24-DSL	5 + Δ*
48	S	17.2	STU-R	256	symmetric	49-DSL	5 + Δ*
49	BT2-R	16.4	STU-R	256	symmetric	49-DSL	5 + Δ*
50	BT2-R	16.4	STU-R	256	symmetric	24-SHDSL + 24-DSL	5 + Δ*
51	S	19.8	STU-C	192	symmetric	49-DSL	5 + Δ*
52	BT2-C	19.1	STU-C	192	symmetric	49-DSL	5 + Δ*
53	BT2-C	19.1	STU-C	192	symmetric	24-DSL + 24 SHDSL	5 + Δ*
54	S	19.8	STU-R	192	symmetric	49-DSL	5 + Δ*
55	BT2-R	19.1	STU-R	192	symmetric	49-DSL	5 + Δ*
56	BT2-R	19.1	STU-R	192	symmetric	24-DSL + 24 SHDSL	5 + Δ*

* The indicated noise margins in Table A-1 shall have a tolerance of 1.25 dB due to the aggregate effect of crosstalk generator tolerance and calibrated loop simulator tolerance. The offset Δ is defined in § A.3.1.4.

All interferers are assumed to be co-located. The notation 24 or 49 SHDSL refers to SHDSL at the same rate and PSD as the system under test. All interferer PSDs are described in § A.3.3.9.

The process for selecting which tests to perform for a specific G.991.2 device under test (DUT) is determined by following each of these 6 steps in order:

1) Determine the set of rates which are in common between the set of supported payload data rates and the following set of payload data rates : (symmetric PSD: 192, 256, 384, 768, 1 544, 2 048, 2 304 kbit/s; asymmetric PSD: 768, 1 544 kbit/s). Call the resulting list of common rates the intersection list.

2) If 1 544 kbit/s asymmetric is in the intersection list, then test the DUT with test cases 1-8 in Table A-1.

3) If 768 kbit/s asymmetric is in the intersection list, then test the DUT with test cases 33-38 in Table A-1.

4) If 1 544 kbit/s symmetric is in the intersection list, then test the DUT with test cases 21-26.

5) For the highest and the lowest symmetric PSD rate in the intersection list, test the DUT with all six cases associated with that rate. For example, if 192 kbit/s symmetric is the lowest rate and 2 304 kbit/s symmetric is the highest rate, then test with test cases 51-56 and 9-14 in Table A-1.

6) For all remaining rates in the intersection list that have not been tested, test using the cases involving only Loop S. For example, if 256, 384, 768, and 2 048 kbit/s symmetric are the remaining rates, then test with the additional test cases 48, 45, 42, 39, 30, 27, 18, and 15.

If all rates are implemented by the DUT, there will be a total of 40 tests.

A.3.2 Impulse Noise Tests

A.3.2.1 Impulse Noise Test Procedure

The impulse noise waveform V(t) (hereafter called the "test impulse") is defined as:

$$V(t) = \begin{cases} K|t|^{-3/4} & t > 0 \\ 0 & t = 0 \\ -K|t|^{-3/4} & t < 0 \end{cases}$$

where t is time given in units of seconds and K is a constant defined numerically in Table A-2. If the pulse is realized using discrete samples of $V(t)$, the waveform should be sampled at $t = (2n-1)\frac{T}{2}$, where T is the sampling period and $(1/T)$ should be at least twice the symbol rate of the system under test. The sampled peak-to-peak amplitude will vary with sampling rate. It can be calculated using the following formula: $V_{p-p} = 2K\left|\frac{T}{2}\right|^{-\frac{3}{4}}$.

TABLE A-2

Impulse noise peak-to-peak voltage requirement

K	$V_{P\text{-}P}$ of the test impulse sampled at 2 Msamples/s
1.775×10^{-6}	320 mV

For a sampling rate of 2 Msamples/s, a minimum of 8 000 samples is required with an amplitude accuracy of at least 12 bits. Figure A-4 shows the test impulse sampled at 2 Msamples/s. The injection circuit shall be identical to that described in § A.3.1.

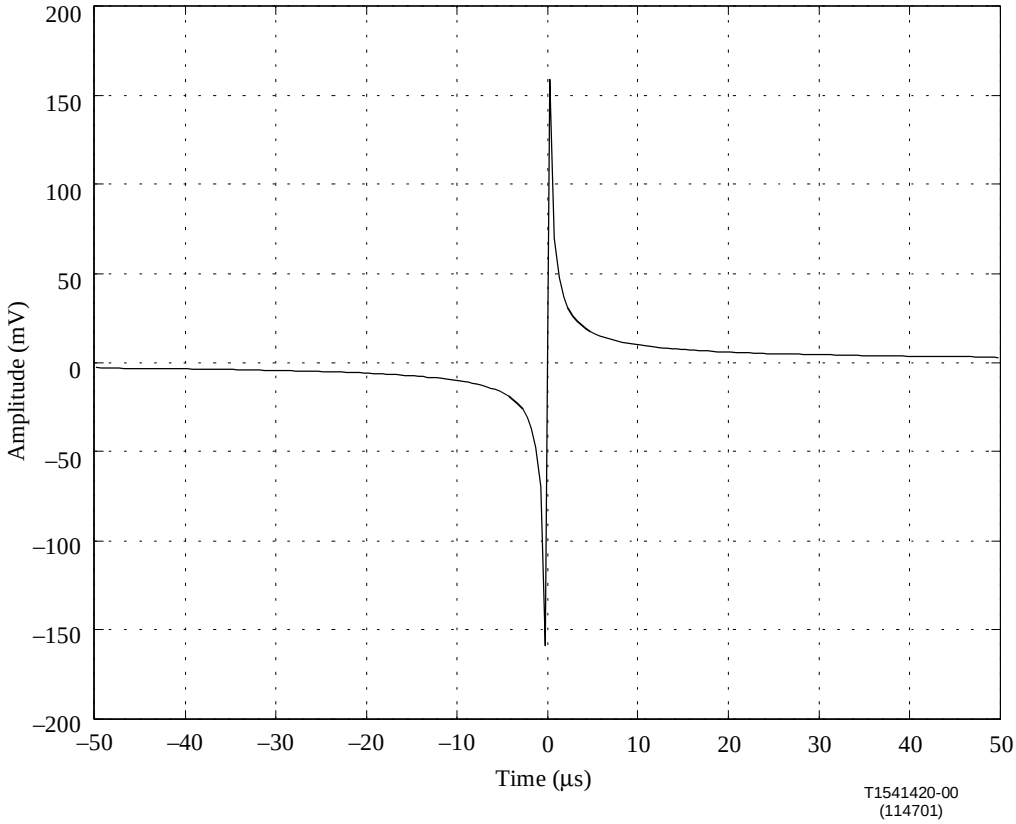


FIGURE A-4

Time Domain Representation of the Test Pulse Sampled at 2 Msamples/s

A.3.2.2 Impulse Noise Test Performance

A compliant unit shall pass the impulse noise test specified in Table A-3. The minimum test period shall be 10 s. Each SHSDL termination shall be tested independently, i.e. the impulse noise waveform is not injected at both terminations simultaneously.

TABLE A-3

Impulse Noise Test Criteria

Test Loop	**Test Pulse V_{P-P} when Sampled at 2 Msamples/s**	**Test Pulse Repetition Rate**	**Bit Error Ratio Upper Limit**
Loop C4	320 mV	10 Hz	5.0×10^{-4}
Loop S, *L* = 9 000'	320 mV	10 Hz	5.0×10^{-4}
NOTE - The entries in this table only correctly apply to the 1 544 kbit/s asymmetric case. Appropriate values for other rates and PSDs are for further study.			

A.3.3 Power Spectral Density of Crosstalk Disturbers

A.3.3.1 Simulated HDSL PSD

The PSD of HDSL disturbers shall be expressed as:

$$PSD_{HDSL} = K_{HDSL} \times \frac{2}{f_0} \times \left[\frac{\sin\left(\frac{\pi f}{f_0}\right)}{\left(\frac{\pi f}{f_0}\right)} \right]^2 \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^8}, \quad f_{3dB} = 196 \text{ kHz}, \ 0 \le f < \infty$$

$$\text{where } f_0 = 392 \text{ kHz}, K_{HDSL} = \frac{5}{9} \times \frac{V_p^2}{R}, V_p = 2.70 \text{ V}, \text{ and } R = 135\,\Omega$$

This equation gives the single-sided PSD; that is, the integral of PSD, with respect to *f*, from 0 to infinity, gives the power in Watts. PSD_{HDSL} is the PSD of a 392 ksymbol/s 2B1Q signal with random equiprobable levels, with full-band square-topped pulses and with 4th order Butterworth filtering (f_{3dB} = 196 kHz).

A.3.3.2 Simulated T1 line PSD

The PSD of the T1 line disturber is assumed to be the 50% duty-cycle random Alternate Mark Inversion (AMI) code at 1.544 Mbit/s. The single-sided PSD shall be expressed as:

$$PSD_{T1} = \frac{V_p^2}{R_L} \times \frac{2}{f_0} \left[\frac{\sin\left(\frac{\pi f}{f_0}\right)}{\frac{\pi f}{f_0}} \right]^2 \sin^2\left(\frac{\pi f}{2 f_0}\right) \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^6} \times \frac{f^2}{f^2 + f_c^2}, \quad 0 \le f < \infty$$

where V_P = 3.6 V, R_L = 100 Ω, and f_O = 1.544 MHz.

The formula assumes that transmitted pulses are passed through a low-pass shaping filter. The shaping filter is chosen as a 3rd order low-pass Butterworth filter with 3 dB point at 3.0 MHz. The filter magnitude squared transfer function is:

$$\left|H_{shaping}(f)\right|^2 = \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^6}$$

The formula also models the coupling transformer as a high-pass filter with 3 dB point at 40 kHz using:

$$\left|H_{Transformer}(f)\right|^2 = \frac{f^2}{f^2 + f_c^2}$$

A.3.3.3 Simulated ADSL Downstream Frequency Division Duplex (FDD) PSD

The ADSL Downstream FDD PSD is based on the ATU-C transmitter PSD mask for reduced NEXT defined in Figure A-2 of ITU-T G.992.1 [1]. The simulated PSD used for SHDSL

performance testing shall be defined as this ITU-T G.992.1 mask reduced by 3.5 dBm/Hz over all frequencies.

A.3.3.4 Simulated ADSL Upstream PSD

The ADSL Upstream PSD is based on the ATU-R transmitter PSD mask defined in Figure A-3 of ITU-T G.992.1 [1]. The simulated PSD used for SHDSL performance testing shall be defined as this ITU-T G.992.1 mask reduced by 3.5 dBm/Hz over all frequencies.

A.3.3.5 Simulated SHDSL Upstream PSD

The SHDSL Upstream PSD masks are defined in § A.4. The simulated PSD used for SHDSL performance testing shall be the worst-case ensemble summation of the nominal upstream PSDs from § A.4, with PBO set to 0 dB. The nominal PSD is given by the expression *NominalPSD(f)* in § A.4.1, § A.4.2, and § A.4.3.

A.3.3.6 Simulated SHDSL Downstream PSD

The SHDSL Downstream PSD masks are defined in § A.4. The simulated PSD used for SHDSL performance testing shall be the worst-case ensemble summation of the nominal downstream PSDs from § A.4, with PBO set to 0 dB. The nominal PSD is given by the expression *NominalPSD(f)* in § A.4.1, § A.4.2, and § A.4.3.

A.3.3.7 Simulated DSL PSD

The power spectral density (PSD) of basic access DSL disturbers is expressed as:

$$PSD_{DSL-Disturber} = K_{DSL} \times \frac{2}{f_0} \times \left[\frac{\sin\left(\frac{\pi f}{f_0}\right)}{\left(\frac{\pi f}{f_0}\right)} \right]^2 \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^4}, \quad f_{3dB} = 80\,\text{kHz},\ 0 \le f < \infty$$

$$\text{where } f_0 = 80\ \text{kHz}, K_{DSL} = \frac{5}{9} \times \frac{V_p^2}{R}, V_p = 2.50\ \text{V}, \text{and } R = 135\,\Omega$$

This equation gives the single-sided PSD; that is, the integral of PSD, with respect to *f*, from 0 to infinity, gives the power in Watts. $PSD_{DSL\text{-}Disturber}$ is the PSD of an 80 ksymbol/sec 2B1Q signal with random equiprobable levels, with full-band square-topped pulses and with 2nd order Butterworth filtering ($f_{3\,dB}$ = 80 kHz).

A.3.3.8 NEXT

The NEXT power transfer function uses the two-piece Unger model which has a slope of 14 dB/decade for frequencies greater than 20 kHz and a slope of 4 dB/decade for frequencies less than or equal to 20 kHz. This is defined as follows where N is the total number of NEXT disturbers:

$$\left|H_{NEXT-2-Piece}(f,N)\right|^2 = \begin{cases} 4.6288 \times 10^{-10} \times f^{0.4} \times N^{0.6}, & f \le 20kHz \\ 2.3144 \times 10^{-14} \times f^{1.4} \times N^{0.6}, & f > 20kHz \end{cases}$$

The two-piece Unger model shall be used to model crosstalk when evaluating performance of the 1.536 or 1.544 Mbps asymmetric PSD.

The one-piece model for NEXT power transfer function is defined as follows where N is the total number of NEXT disturbers:

$$\left|H_{NEXT-1-Piece}(f,N)\right|^2 = 0.8536\times10^{-14}\times f^{1.5}\times N^{0.6}$$

The one-piece model shall be used to model crosstalk when evaluating performance for all rates and PSDs except the 1.536 or 1.544 Mbps asymmetric PSD.

The model for FEXT power transfer function is defined as follows where N is the total number of FEXT disturbers:

$$\left|H_{FEXT}(f,N,L,D)\right|^2 = \left|L(f)\right|^2 \times D\times 7.744\times10^{-21}\times f^2\times N^{0.6}$$

where L(f) is the insertion loss of the loop through which the interferer passes while the interferer and the signal under test are adjacent in the same binder, and D is the length of the loop in feet. The FEXT model shall be used to model crosstalk from asymmetric interferers (specifically 1.544 Mbps asymmetric and ADSL).

A.3.3.9 Crosstalk PSD Definitions

The following PSD definitions are to be used to generate the crosstalk interferer combinations used for performance testing in Table A-1.

$$PSD_{Case-1} = \frac{24\times PSD_{T1}(f) + 24\times PSD_{SHDSL-1544-Asym-Down}(f)}{48}\times\left|H_{NEXT-2-Piece}(f,48)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f)\times\left|H_{FEXT}(f,24,L_{C4},7600)\right|^2$$

$$PSD_{Case-2} = PSD_{SHDSL-1544-Asym-Down}(f)\times\left|H_{NEXT-2-Piece}(f,39)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f)\times\left|H_{FEXT}(f,39,L_{C4},7600)\right|^2$$

$$PSD_{Case-3} = \frac{24\times PSD_{ADSL-Down}(f) + 24\times PSD_{HDSL}(f)}{48}\times\left|H_{NEXT-2-Piece}(f,48)\right|^2 + PSD_{ADSL-Up}(f)\times\left|H_{FEXT}(f,24,L_{C4},7600)\right|^2$$

$$PSD_{Case-4} = \frac{24\times PSD_{T1}(f) + 24\times PSD_{SHDSL-1544-Asym-Down}(f)}{48}\times\left|H_{NEXT-2-Piece}(f,48)\right|^2 + PSD_{ADSL-1544-Asym-Up}(f)\times\left|H_{FEXT}(f,24,L_{S9.0},9000)\right|^2$$

$$PSD_{Case-5} = PSD_{SHDSL-1544-Asym-Down}(f)\times\left|H_{NEXT-2-Piece}(f,39)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f)\times\left|H_{FEXT}(f,39,L_{S9.0},9000)\right|^2$$

$$PSD_{Case-6} = \frac{24\times PSD_{ADSL-Down}(f) + 24\times PSD_{HDSL}(f)}{48}\times\left|H_{NEXT-2-Piece}(f,48)\right|^2 + PSD_{ADSL-Up}(f)\times\left|H_{FEXT}(f,24,L_{S9.0},9000)\right|^2$$

$$PSD_{Case-7} = \frac{24\times PSD_{T1}(f) + 24\times PSD_{SHDSL-1544-Asym-Up}(f)}{48}\times\left|H_{NEXT-2-Piece}(f,48)\right|^2 + PSD_{SHDSL-1544-Asym-Down}(f)\times\left|H_{FEXT}(f,24,L_{C4},7600)\right|^2$$

$$PSD_{Case-8} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times \left|H_{NEXT-2-Piece}(f,48)\right|^2 + PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{FEXT}(f,24,L_{S9.0},9000)\right|^2$$

$$PSD_{Case-9} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Down}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f,24,L_{S6.3},6300)\right|^2$$

$$PSD_{Case-10} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Down}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f,24,L_{BT1-C5.2},5200)\right|^2$$

$$PSD_{Case-11} = PSD_{SHDSL-2304-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-12} = PSD_{SHDSL-2304-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-13} = PSD_{SHDSL-2304-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-14} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{FEXT}(f,24,L_{BT1-R5.2},5200)\right|^2$$

$$PSD_{Case-15} = \frac{24 \times PSD_{ADSL-Down}(f) + 24 \times PSD_{SHDSL-2048-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + PSD_{ADSL-Up}(f) \times \left|H_{FEXT}(f,24,L_{S6.8},6800)\right|^2$$

$$PSD_{Case-16} = PSD_{SHDSL-2048-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-17} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Down}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f,24,L_{BT1-C5.6},5600)\right|^2$$

$$PSD_{Case-18} = PSD_{SHDSL-2048-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-19} = PSD_{SHDSL-2048-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-20} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{FEXT}(f,24,L_{BT1-R5.6},5600)\right|^2$$

$$PSD_{Case-21} = PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{NEXT-1-Piece}(f,39)\right|^2 + PSD_{SHDSL-1544-Asym-Up}(f) \times \left|H_{FEXT}(f,39,L_{S7.9},7900)\right|^2$$

$$PSD_{Case-22} = \frac{24 \times PSD_{ADSL-Down}(f) + 24 \times PSD_{SHDSL-1544-Asym-Down}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + \frac{24 \times PSD_{ADSL-Up}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times \left|H_{FEXT}(f,48,L_{BT1-C6.4},6400)\right|^2$$

$$PSD_{Case-23} = \frac{24 \times PSD_{ADSL-Down}(f) + 24 \times PSD_{SHDSL-1544-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + PSD_{ADSL-Up}(f) \times \left|H_{FEXT}(f,24,L_{BT1-C6.4},6400)\right|^2$$

$$PSD_{Case-24} = PSD_{SHDSL-1544-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-25} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-1544-Asym-Up}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + PSD_{SHDSL-1544-Asym-Down}(f) \times \left|H_{FEXT}(f,24,L_{BT1-R6.4},6400)\right|^2$$

$$PSD_{Case-26} = PSD_{SHDSL-1544-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-27} = PSD_{HDSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-28} = PSD_{SHDSL-768-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-29} = PSD_{HDSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-30} = PSD_{HDSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-31} = PSD_{SHDSL-768-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-32} = PSD_{HDSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-33} = PSD_{HDSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-34} = PSD_{HDSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-35} = \frac{24 \times PSD_{ADSL-Down}(f) + 24 \times PSD_{HDSL}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + PSD_{ADSL-Up}(f) \times \left|H_{FEXT}(f,24,L_{BT1-C10.4},10400)\right|^2$$

$$PSD_{Case-36} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{HDSL}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2$$

$$PSD_{Case-37} = \frac{24 \times PSD_{T1}(f) + 24 \times PSD_{SHDSL-768-Asym-Up}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2 + PSD_{SHDSL-768-Asym-Down}(f) \times \left|H_{FEXT}(f,24,L_{BT1-R10.4},10400)\right|^2$$

$$PSD_{Case-38} = PSD_{ADSL-Up}(f) \times \left|H_{NEXT-1-Piece}(f,39)\right|^2 + PSD_{ADSL-Down}(f) \times \left|H_{FEXT}(f,39,L_{BT1-R10.4},10400)\right|^2$$

$$PSD_{Case-39} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-384-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2$$

$$PSD_{Case-40} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-384-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2$$

$$PSD_{Case-41} = PSD_{SHDSL-384-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-42} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-384-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2$$

$$PSD_{Case-43} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-384-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2$$

$$PSD_{Case-44} = PSD_{SHDSL-384-Sym}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-45} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-46} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-47} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-256-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2$$

$$PSD_{Case-48} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-49} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-50} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-256-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2$$

$$PSD_{Case-51} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-52} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-53} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-192-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2$$

$$PSD_{Case-54} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-55} = PSD_{DSL}(f) \times \left|H_{NEXT-1-Piece}(f,49)\right|^2$$

$$PSD_{Case-56} = \frac{24 \times PSD_{DSL}(f) + 24 \times PSD_{SHDSL-192-Sym}(f)}{48} \times \left|H_{NEXT-1-Piece}(f,48)\right|^2$$

A.4 PSD Masks

For all data rates, the measured transmit PSD of each STU shall not exceed the PSD masks specified in this section ($PSDMASK_{SHDSL}(f)$), and the measured total power into 135 Ω shall fall within the range specified in this section ($P_{SHDSL} \pm 0.5$ dB).

Support for the symmetric PSDs specified in § A.4.1 shall be mandatory for all supported data rates. Support for the asymmetric PSDs specified in § A.4.2 and § A.4.3 shall be optional.

A.4.1 Symmetric PSD Masks

For all values of framed data rate available in the STU, the following set of PSD masks ($PSDMASK_{SHDSL}(f)$) shall be selectable:

$$PSDMASK_{SHDSL}(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \frac{K_{SHDSL}}{135} \times \frac{1}{f_{sym}} \times \frac{\left[\sin\left(\frac{\pi f}{N f_{sym}}\right)\right]^2}{\left(\frac{\pi f}{N f_{sym}}\right)^2} \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^{2\times Order}} \times 10^{\frac{MaskedOffsetdB(f)}{10}}, & f < f_{\text{int}} \\ 0.5683\times 10^{-4} \times f^{-1.5}, & f_{\text{int}} \le f \le 1.1MHz \end{cases}$$

where *MaskOffsetdB(f)* is defined as

$$MaskOffsetdB(f) = \begin{cases} 1+0.4\times\frac{f_{3dB}-f}{f_{3dB}}, & f < f_{3dB} \\ 1, & f \ge f_{3dB} \end{cases}$$

f_{int} is the frequency where the two functions governing $PSDMASK_{\text{SHDSL}}(f)$ intersect in the range 0 to f_{sym}. PBO is the power backoff value in dB. K_{SHDSL}, *Order*, *N*, f_{sym}, $f_{3\text{dB}}$, and P_{SHDSL} are defined in Table A-4. P_{SHDSL} is the range of power in the transmit PSD with 0 dB power backoff. *R* is the payload data rate.

TABLE A-4

Symmetric PSD parameters

Payload Data Rate, *R* (kbit/s)	K_{SHDSL}	***Order***	***N***	f_{sym} **(ksymbol/s)**	$f_{3\text{dB}}$	P_{SHDSL} **(dBm)**
R < 1 536	7.86	6	1	(R+8)/3	1.0xf_{sym}/2	$P1(R) \le P_{\text{SHDSL}} \le 13.5$
1 536 or 1 544	8.32	6	1	(R+8)/3	0.9xf_{sym}/2	13.5
R > 1 544	7.86	6	1	(R+8)/3	1.0xf_{sym}/2	13.5

$P1(R)$ is defined as follows:

$$P1(R) = 0.3486\log_2(R\times 1\,000 + 8\,000) + 6.06 \text{ dBm}$$

For 0 dB power backoff, the measured transmit power into 135 Ω shall fall within the range P_{SHDSL}±0.5 dB. For power backoff values other than 0 dB, the measured transmit power into 135 Ω shall fall within the range P_{SHDSL}±0.5 dB minus the power backoff value in dB. The measured transmit PSD into 135 Ω shall remain below $PSDMASK_{\text{SHDSL}}(f)$.

Figure A-5 shows the PSD masks with 0 dB power backoff for payload data rates of 256, 512, 768, 1 536, 2 048 and 2 304 kbit/s.

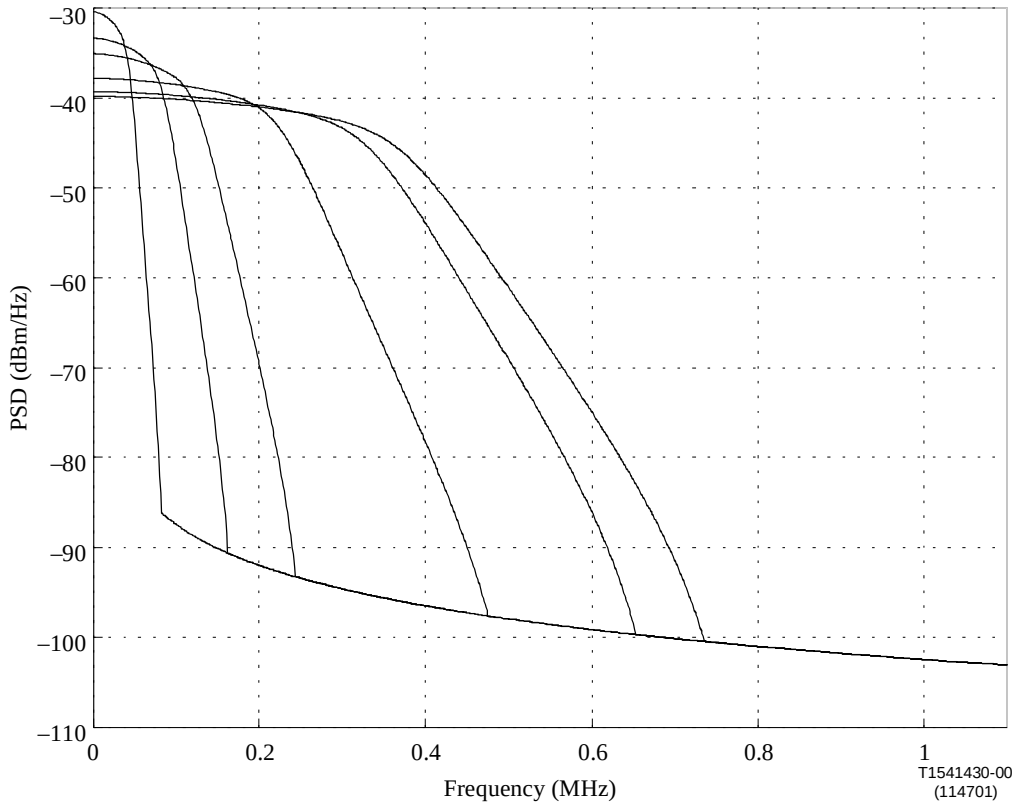


FIGURE A-5

PSD Masks for 0 dB Power Backoff

The equation for the nominal PSD measured at the terminals is:

$$NominalPSD(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \frac{K_{SHDSL}}{135} \times \frac{1}{f_{sym}} \times \frac{\left[\sin\left(\frac{\pi f}{N f_{sym}}\right)\right]^2}{\left(\frac{\pi f}{N f_{sym}}\right)^2} \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^{2\times Order}} \times \frac{f^2}{f^2 + f_c^2}, & f < f_{\text{int}} \\ 0.5683\times 10^{-4} \times f^{-1.5}, & f_{\text{int}} \le f \le 1.1MHz \end{cases}$$

where f_c is the transformer cut-off frequency, assumed to be 5 kHz. Figure A-6 shows the nominal transmit PSDs with 13.5 dBm power for payload data rates of 256, 512, 768, 1 536, 2 048 and 2 304 kbit/s. NOTE - The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations (see § A.3.3.5 and § A.3.3.6) as representative of typical implementations.

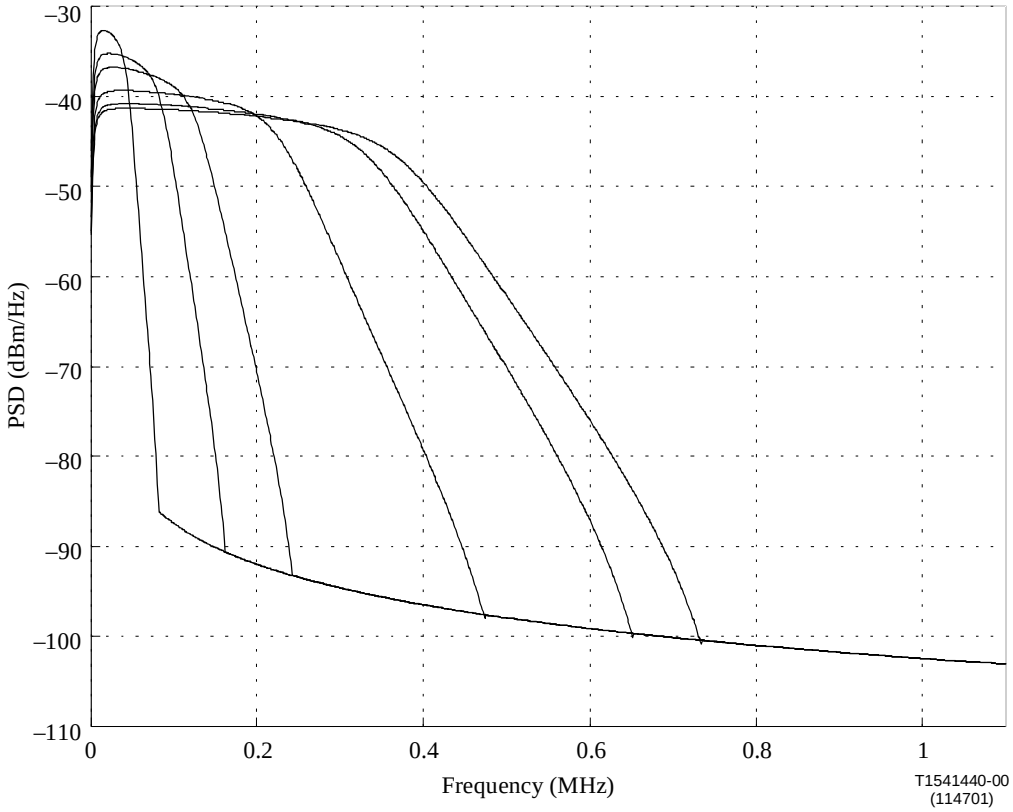


FIGURE A-6

Nominal PSDs for 0 dB Power Backoff

NOTE: In this section, *PSDMASK(f)* and *NominalPSD(f)* are in units of W/Hz, and *f* is in units of Hz.

A.4.2 Asymmetric 1.536 or 1.544 PSD Mask

The asymmetric PSD mask set specified in § A.4.2.1 and § A.4.2.2 shall optionally be supported for 1.536 and 1.544 Mbit/s payload data rates (1.544 and 1.552 Mbit/s framed data rates) in North America. The PSD masks are described for the 0 dB power backoff case. For other values of power backoff, the passband PSD masks shall shift, but the out-of-band mask shall remain constant. Power and power spectral density is measured into a load impedance of 135 Ω.

A.4.2.1 PSD Mask for STU-C

For 0 dB power backoff, the output power of the STU-C during data mode shall be (16.8 ± 0.5) dBm in the frequency band from 0 to 440 kHz and shall be limited by the mask of Figure A-7. Table A-5 provides the numerical values for the mask of Figure A-7. The PSD mask is created by linear interpolation of the frequency and power (dBm/Hz) entries of Table A-5.

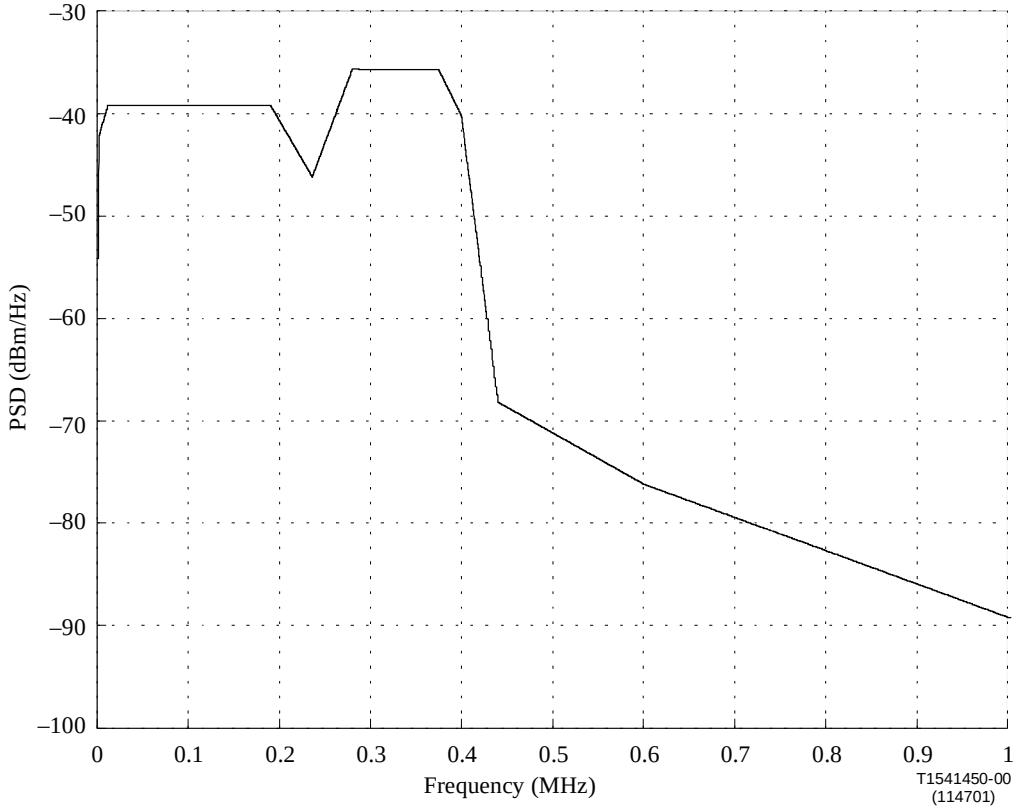


FIGURE A-7

STU-C PSD Mask for 1.536 or 1.544 Mbit/s with 0 dB Power Backoff

TABLE A-5

STU-C PSD Mask Values for 1.536 or 1.544 Mbit/s with 0 dB Power Backoff

Frequency (kHz)	**Maximum Power (dBm/Hz)**	**Frequency (kHz)**	**Maximum Power (dBm/Hz)**	**Frequency (kHz)**	**Maximum Power (dBm/Hz)**
≤1	–54.2 - *PBO*	280	–35.7 - *PBO*	1 000	–89.2
2	–42.2 - *PBO*	375	–35.7 - *PBO*	2 000	–99.7
12	–39.2 - *PBO*	400	–40.2 - *PBO*	≥3 000	–108
190	–39.2 - *PBO*	440	–68.2		
236	–46.2 – *PBO*	600	–76.2		

The STU-C PSD mask shall be calculated by subtracting *PBO* (the Power Backoff value, in dB) from each PSD value in Table A-5 for frequencies less than or equal to 400 kHz, then by linear interpolation of the frequency and power (dBm/Hz) over all frequencies. The output power of the STU-C during data mode shall be (16.8 - *PBO* ± 0.5) dBm in the frequency band from 0 to 440 kHz. The power level during start-up shall be (16.6 - *PBO* ± 0.5) dBm. The nominal PSD (*NominalPSD(f)*) is defined as the PSD mask with PBO set to 1 dB. NOTE - The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations (see § A.3.3.5 and § A.3.3.6) as representative of typical implementations.

A.4.2.2 PSD Mask for STU-R

For 0 dB power backoff, the output power of the STU-R during data mode shall be (16.5 ± 0.5) dBm in the frequency band from 0 to 300 kHz and shall be limited by the mask of Figure A-8. Table A-6 provides the numerical values for the mask of Figure A-8. The PSD mask is created by linear interpolation of the frequency and power (dBm/Hz) entries of Table A-6.

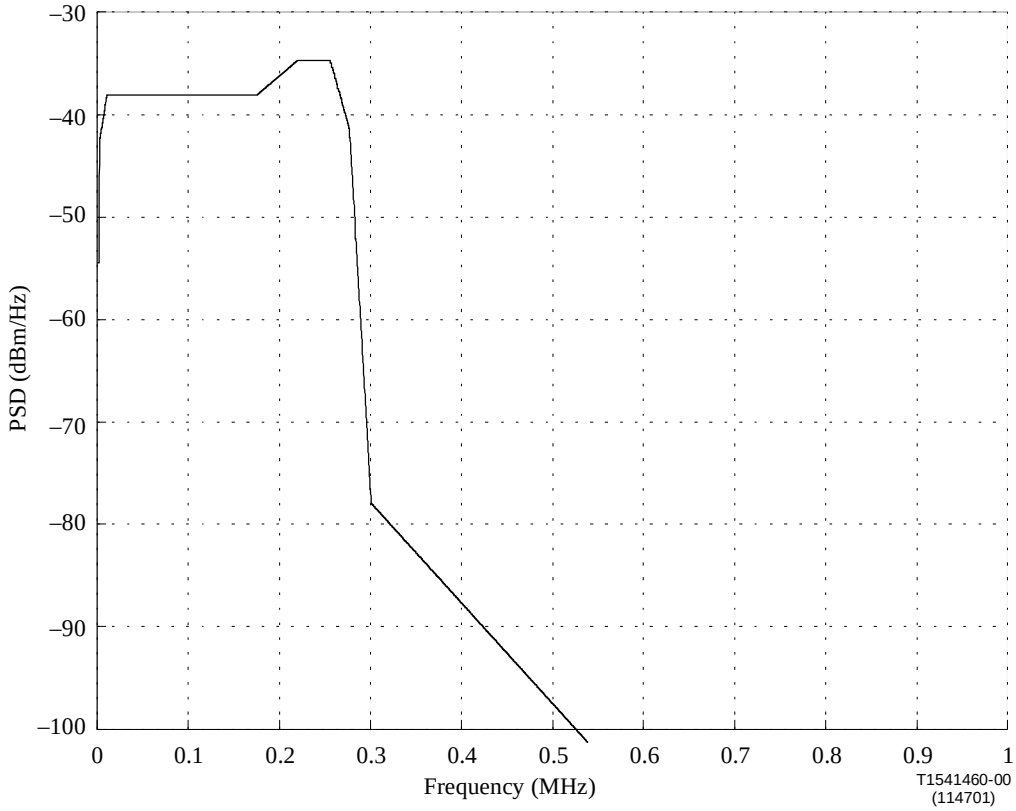


FIGURE A-8

STU-R PSD Mask for 1.536 or 1.544 Mbit/s with 0 dB Power Backoff

TABLE A-6

STU-R PSD Mask Values for 1.536 or 1.544 Mbit/s with 0 dB Power Backoff

Frequency (kHz)	Maximum Power (dBm/Hz)	Frequency (kHz)	Maximum Power (dBm/Hz)	Frequency (kHz)	Maximum Power (dBm/Hz)
≤1	–54.2 - PBO	220	–34.4 - PBO	555	–102.6
2	–42.1 - PBO	255	–34.4 - PBO	800	–105.6
10	–37.8 - PBO	276	–41.1 - PBO	1 400	–108
175	–37.8 - PBO	300	–77.6	≥2 000	–108

The STU-R PSD mask shall be calculated by subtracting *PBO* (the Power Backoff value, in dB) from each PSD value in Table A-6 for frequencies less than or equal to 276 kHz, then by linear interpolation of the frequency and power (dBm/Hz) over all frequencies. The output power of the STU-R during data mode shall be (16.5 - *PBO* ± 0.5) dBm in the frequency band from 0 to 300 kHz. The power level during start-up shall be (16.3 - *PBO* ± 0.5) dBm. The nominal PSD (*NominalPSD(f)*) is defined as the PSD mask with PBO set to 1 dB. NOTE - The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations (see § A.3.3.5 and § A.3.3.6) as representative of typical implementations.

A.4.3 Asymmetric PSD Masks for 768 or 776 kbit/s data rates

The asymmetric PSD mask set specified in § A.4.3.1 and § A.4.3.2 shall optionally be supported for the 768 kbit/s and 776 kbit/s payload data rates (776 and 784 kbit/s framed data rates) in North America. The PSD masks are described for the 0 dB power backoff case. For other values of power backoff, the passband PSD masks shall shift, but the out-of-band mask shall remain constant. Power and power spectral density is measured into a load impedance of 135 Ω.

A.4.3.1 PSD Mask for STU-C

For 0 dB power backoff, the output power of the STU-C during data mode shall be (14.1 ± 0.5) dBm in the frequency band from 0 to 600 kHz and shall be limited by the mask of Figure A-9. Table A-7 provides the numerical values for the mask of Figure A-9. The PSD mask is created by linear interpolation of the frequency and power (dBm/Hz) entries of Table A-7.

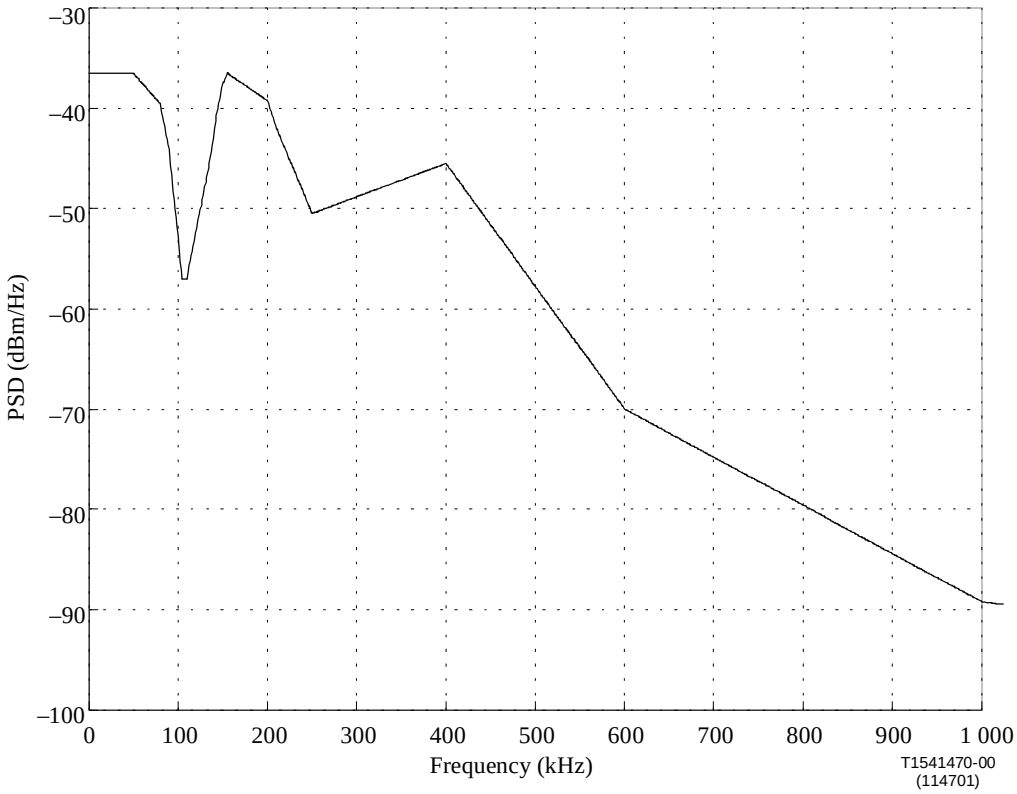


FIGURE A-9

STU-C PSD Mask for 768 or 776 kbit/s with 0 dB Power Backoff

TABLE A-7

STU-C PSD Mask Values for 768 or 776 kbit/s with 0 dB Power Backoff

Frequency (kHz)	Maximum Power (dBm/Hz)	Frequency (kHz)	Maximum Power (dBm/Hz)	Frequency (kHz)	Maximum Power (dBm/Hz)
≤50	–36.5 - *PBO*	135	–45.5 - *PBO*	250	–50.5 - PBO
80	–39.5 - *PBO*	145	–39.5 - *PBO*	400	–45.5 - PBO
90	–44 - *PBO*	150	–37.5 - *PBO*	600	–70
105	–57 - *PBO*	155	–36.5 - PBO	1 000	–89.2
110	–57 - *PBO*	200	–39.25 - PBO	2 000	–99.7
		210	–42 - PBO	≥3 000	–108

The STU-C PSD mask shall be calculated by subtracting *PBO* (the Power Backoff value, in dB) from each PSD value in Table A-7 for frequencies less than or equal to 400 kHz, then by linear interpolation of the frequency and power (dBm/Hz) over all frequencies. The output power of the STU-C during data mode shall be (14.1 - *PBO* ± 0.5) dBm in the frequency band from 0 to 600 kHz. The power level during start-up shall be (13.9 - *PBO* ± 0.5) dBm. The nominal PSD (*NominalPSD(f)*) is defined as the PSD mask with PBO set to 1 dB, multiplied by $f^2/(f^2+f_c^2)$ where f is the frequency in Hz and f_c is 5 000 Hz, the nominal transformer cut-off frequency. NOTE - The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations (see § A.3.3.5 and § A.3.3.6) as representative of typical implementations.

A.4.3.2 PSD Mask for STU-R

For 0 dB power backoff, the output power of the STU-R during data mode shall be (14.1 ± 0.5) dBm in the frequency band from 0 to 300 kHz and shall be limited by the mask of Figure A-10. Table A-8 provides the equations for the mask of Figure A-10.

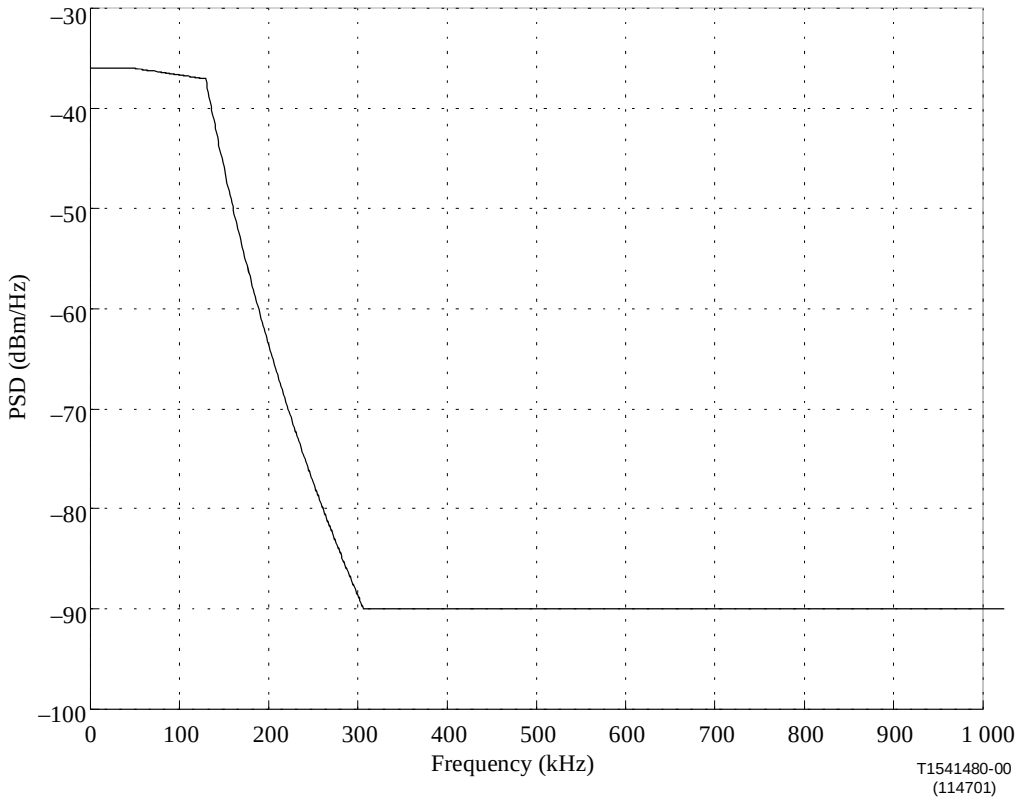


FIGURE A-10

STU-R PSD Mask for 768 or 776 kbit/s with 0 dB Power Backoff

TABLE A-8

STU-R PSD Mask Values for 768 or 776 kbit/s with 0 dB Power Backoff

Frequency, *f* (Hz)	**Maximum Power (dBm/Hz)**
$0 < f \leq 50\,000$	–36 - PBO
$50\,000 < f \leq 125\,000$	–36 - PBO - ((f-50 000)/75 000)
$125\,000 < f \leq 130\,000$	–37 - PBO
$130\,000 < f \leq 307\,000$	–37 - PBO - $142\log_{10}(f/130\,000)$
$307\,000 < f \leq 1\,221\,000$	–90
$1\,221\,000 < f \leq 1\,630\,000$	–90 peak, with max power in the [f, f + 1 MHz] window of (–90 - $48\log_2(f/1\,221\,000)$ + 60) dBm
$f > 1\,630\,000$	–90 peak, with max power in the [f, f+1MHz] window of –50 dBm

The STU-R PSD mask shall be calculated by subtracting *PBO* (the Power Backoff value, in dB) from each PSD value in Table A-8 for frequencies less than or equal to 307 kHz, then by evaluation of the equations for power (dBm/Hz) over all frequencies. The output power of the STU-R during

data mode shall be (14.1 - *PBO* ± 0.5) dBm in the frequency band from 0 to 307 kHz. The power level during start-up shall be (13.9 - *PBO* ± 0.5) dBm. The nominal PSD (*NominalPSD(f)*) is defined as the PSD mask with PBO set to 1 dB, multiplied by $f^2/(f^2+f_c^2)$ where f is the frequency in Hz and f_c is 5 000 Hz, the nominal transformer cut-off frequency. NOTE - The nominal PSD is intended to be informative in nature; however, it is used for purposes of crosstalk calculations (see § A.3.3.5 and § A.3.3.6) as representative of typical implementations.

A.5 Region-Specific Functional Characteristics

A.5.1 Data Rate

The operation of the STU in data mode at the specified information rate shall be as specified in Table A-9.

TABLE A-9

Framed Data Mode Rates

Payload Data Rate, *R* (kbit/s)	**Modulation**	**Symbol Rate (ksymbol/s)**	***K*** **(Bits per Symbol)**
$R=n\times64+(i)\times8$	16-TCPAM	$(R+8)\div3$	3

For devices supporting Annex A functionality, no additional limitation on data rates shall be placed beyond the limitations stated in § 5 and reiterated in § 7.1.1, § 8.1 and § 8.2.

A.5.2 Return Loss

For devices supporting Annex A functionality, return loss shall be specified based on the methodology of § 11.3 and the limitations of Figure 11-6. The following definitions shall be applied to the quantities shown in Figure 11-6:

$$RL_{MIN} = 12 \text{ dB}$$
$$f_0 = 12.56 \text{ kHz}$$
$$f_1 = 50 \text{ kHz}$$
$$f_2 = f_{sym}/2$$
$$f_3 = 1.99f_{sym}$$

where f_{sym} is the symbol rate.

A.5.3 Span Powering

The capability for an STU-C to provide power over a span to an STU-R is optional. However, if this capability is provided, the STU-C shall meet the requirements of § A.5.3.1. The capability for an STU-R (or an SRU) to be remotely powered over the span is optional. However, if this capability is provided, the STU-R or SRU shall meet the requirements of § A.5.3.2. Segments that do not support span powering or that have it disabled may optionally provide wetting (sealing) current, as defined in § A.5.3.3.

The STU-C, STU-R and SRU shall comply with all applicable industry safety standards that are consistent with their deployment. In particular, it is highly desirable that SHDSL equipment comply with ITU-T K.50 [B4].

If an STU-R is deployed as CPE (i.e. it is part of a subscriber's installation), then span powering shall be disabled at the STU-C. The STU-C may optionally provide wetting current, as specified in § A.5.3.3.

When implemented, SHDSL span powering shall support DC powering of remote terminal units over single-span loop resistances from 0 to 1 800 Ω. The maximum span resistance shall include the worst-case loop resistance plus the wiring inside the central office and remote site. The STU-C span power supply shall be designed as a voltage source and shall be considered a voltage-limited circuit in the application of all referenced standards.

The span powering requirements defined herein are intended for use across a single segment from an STU-C to either an STU-R or an SRU. Application of these requirements in the STU-C to SRU case shall result in the termination of span powering voltages at the SRU. Succeeding segments may optionally support wetting current. Powering across multiple spans is not prohibited; however, the requirements are for further study. Wetting current may optionally be supported across any segment (STU-R to STU-C, STU-C to SRU, SRU to STU-R or SRU to SRU-R).

To ensure interoperability and reliable operation, the STU-C and STU-R (or SRU) shall meet the following requirements when span powering is implemented:

A.5.3.1 STU-C Span Powering Source

A.5.3.1.1 Output Voltage

The maximum potential between tip and ring shall be 200 V. The minimum potential between tip and ring shall be 160 V.

A.5.3.1.2 Power

The minimum steady-state power output capability shall be 15 W.

A.5.3.1.3 Polarity

The negative potential shall be applied to the terminal designated "ring" or "R". The potential from tip-to-ground should be zero or negative.

A.5.3.1.4 Slew Rate

The supply voltage power-up slew rate at the STU-C loop interface (rise time of V_{TEST}) shall be at least 1 V/ms but no greater than 30 V/ms when measured in the test circuit of Figure A-11 under all test conditions defined in Table A-10.

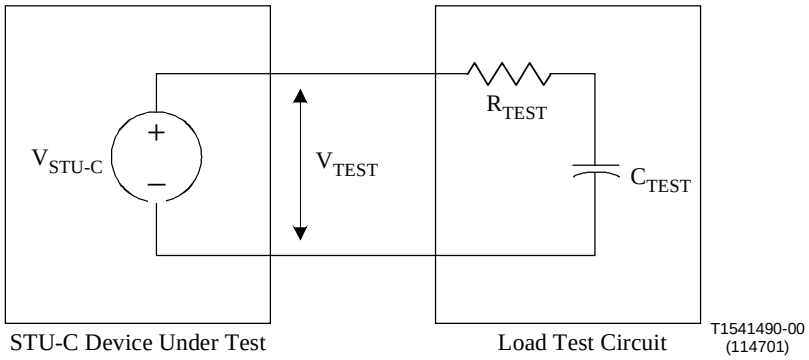


FIGURE A-11

STU-C Power-up Slew Rate Test Circuit

TABLE A-10

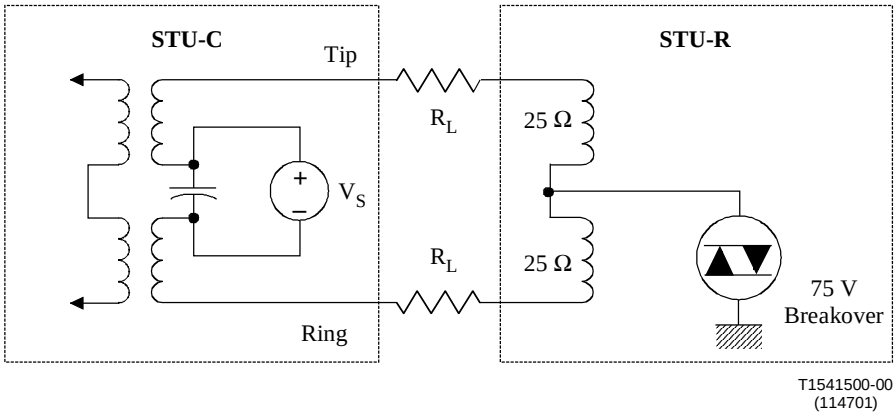
Test Conditions for STU-C Slew Rate

C_{TEST} (µF)	R_{TEST} (Ω)
1.0	100
1.0	1 800
15	100
15	1 800

NOTE (informative) - On a 900 Ω loop, the STU-C output voltage specification results in a maximum remote power load of 7.1 W.

A.5.3.1.5 Power Feeding Oscillation

The STU-C power supply should be designed to ensure that power feeding oscillation (a condition that could result in excessive noise coupling into other wire pairs in the cable) does not occur for the electrical characteristics shown for the protection circuit in Figure A-12.



NOTE (informative) - With appropriate current (to ground) restrictions, these requirements are not in conflict with the criteria of the Class 2 Voltage limits contained in [B5].

FIGURE A-12

Power Oscillation Example Circuit

A.5.3.2 STU-R (and SRU) Powering

A.5.3.2.1 Input Voltage

The STU-R (or SRU) shall operate properly over the range of input voltages from 80 V to 200 V. The STU-R (or SRU) may operate with input voltages less than 80 V.

A.5.3.2.2 Polarity

An STU-R (or SRU) shall function normally independent of the polarity of the line power input voltage. Note that tip/ring reversal is indicated via the EOC by the Maintenance Status Response message (§ 9.5.5.7.20).

A.5.3.2.3 Capacitance

The capacitance of the STU-R (or SRU) shall be less than or equal to 15 μF.

A.5.3.2.4 Load Characteristic

In order to guarantee power system stability during power-up and steady-operation, STU-R (or SRU) shall present a load characteristic which produces the following observable measurements when inserted in the test circuit shown in Figure A-13.

While V_{LINE} is ramped up from 0 V to the specified maximum voltage at the specified slew rate, the values of V_{LINE} and V_{LOAD} shall be observed and recorded. Set t_0 as the recorded time point during the power-up sequence when $V_{LOAD} = V_{LINE}/2$. The load characteristic of the STU-R (or SRU) device under test (DUT) shall be such that for all time $t > t_0$, $V_{LOAD} > V_{LINE}/2$. This criteria shall be met for all test conditions defined in Table A-11.

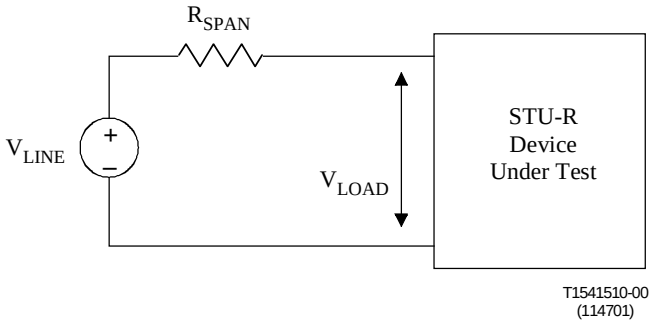


FIGURE A-13

Test Circuit for STU-R Turn-on Load Characteristic

TABLE A-11

Test Conditions for STU-R Turn-on Load Characteristic

V_{LINE} slew rate (V/ms)	V_{LINE} Maximum Voltage	R_{SPAN} (Ω)
1.0	200	100
1.0	160	1 800
30.0	200	100
30.0	160	1 800

The test power supply used to generate V_{LINE} should have a minimum load capacity of 20 W at all output voltages up to 200 V. The test power supply should use linear voltage regulation to minimize transient output voltage effects (observed at V_{LINE}) in the presence of test load variations.

A.5.3.3 Wetting Current

The STU-R (or SRU-R) shall be capable of drawing between 1.0 and 20 mA of wetting (sealing) current from the remote feeding circuit when span powering is disabled or is not supported. The maximum rate of change of the wetting current shall be no more than 20 mA per second.

The STU-C (or SRU-C) may optionally supply power to support wetting current if span powering is disabled or not supported. When enabled, this power source should provide a nominal 48 V (measured from ring to tip). The maximum voltage of the power source (if provided) should be limited to 56.5 V, and the minimum voltage should be high enough to ensure a minimum of 32 V at the inputs of the STU-R or SRU-R. In no case shall the wetting current source apply a voltage greater than 72 V (measured from ring to tip). The potential from tip to ground should be zero or negative.

A.5.3.4 Metallic Termination

A metallic termination at the STU-R shall be provided in conjunction with the use of wetting current (§ A.5.3.3). The SRU-R shall meet the same requirements specified in this section for an STU-R.

Table A-12 and Figure A-14 give characteristics that apply to the DC metallic termination of the STU-R. The metallic termination provides a direct current path from tip to ring at the STU-R,

providing a path for sealing current. By exercising the non-linear functions of the metallic termination, a network-side test system may identify the presence of a conforming STU-R on the customer side of the interface. The characteristics of the metallic termination shall not be affected by whether the STU-R is powered in any state, or unpowered.

There are two operational states of the DC metallic termination:

a) the ON or conductive state; and

b) the OFF or non-conductive state.

A.5.3.4.1 ON State

The application of a voltage across the metallic termination greater than V_{AN}, the activate/non-activate voltage, for a duration greater than the activate time shall cause the termination to transition to the ON state. The activate/non-activate voltage shall be in the range of 30.0 to 39.0 V. The activate time shall be in the range of 3.0 to 50.0 ms. If a change of state is to occur, the transition shall be completed within 50 ms from the point where the applied voltage across the termination first exceeds V_{AN}. Application of a voltage greater than V_{AN} for a duration less than 3.0 ms shall not cause the termination to transition to the ON state. See Table A-12 and Figure A-14.

While in the ON state, when the voltage across the termination is 15 V, the current shall be greater than or equal to 20 mA. The metallic termination shall remain in the ON state as long as the current is greater than the threshold I_{HR} (see Table A-12 and Figure A-14) whose value shall be in the range of 0.1 to 1.0 mA. Application of 90.0 V through 200 to 4 000 Ω (for a maximum duration of 2 s) shall result in a current greater than 9.0 mA.

A.5.3.4.2 OFF State

The metallic termination shall transition to the OFF state if the current falls below the threshold I_{HR} whose value shall be in the range of 0.1 to 1.0 mA for a duration greater than the "guaranteed release" time (100 ms) (see Table A-12 and Figure A-14). If a change of state is to occur, the transition shall be completed within 100 ms from the point where the current first falls below I_{HR}. If the current falls below I_{HR} for a duration less than 3.0 ms, the termination shall not transition to the OFF state. While in the OFF state, the current shall be less than 5.0 µA whenever the voltage is less than 20.0 V. The current shall not exceed 1.0 mA while the voltage across the termination remains less than the activate voltage.

Descriptive material can be found in Table A-12 and Figure A-14.

A.5.3.4.3 STU-R Capacitance

While the metallic termination is OFF, the tip-to-ring capacitance of the STU-R when measured at a frequency of less than 100 Hz shall be 1.0 µF ± 10%.

A.5.3.4.4 Behaviour of the STU-R During Metallic Testing

During metallic testing, the STU-R shall behave as follows:

a) when a test voltage of up to 90 V[2] is applied across the loop under test, the STU-R shall present its DC metallic termination as defined in § A.5.3.4, Table A-12, and Figure A-14, and not trigger any protective device that will mask this signature. The series resistance

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[2] One test system in common use today applies 70 V DC plus 10 Vrms AC (84.4 V peak) to one conductor of the loop while grounding the other conductor.

(test system + test trunk + loop + margin) can be from 200 to 4 000 Ω (balanced between the two conductors);

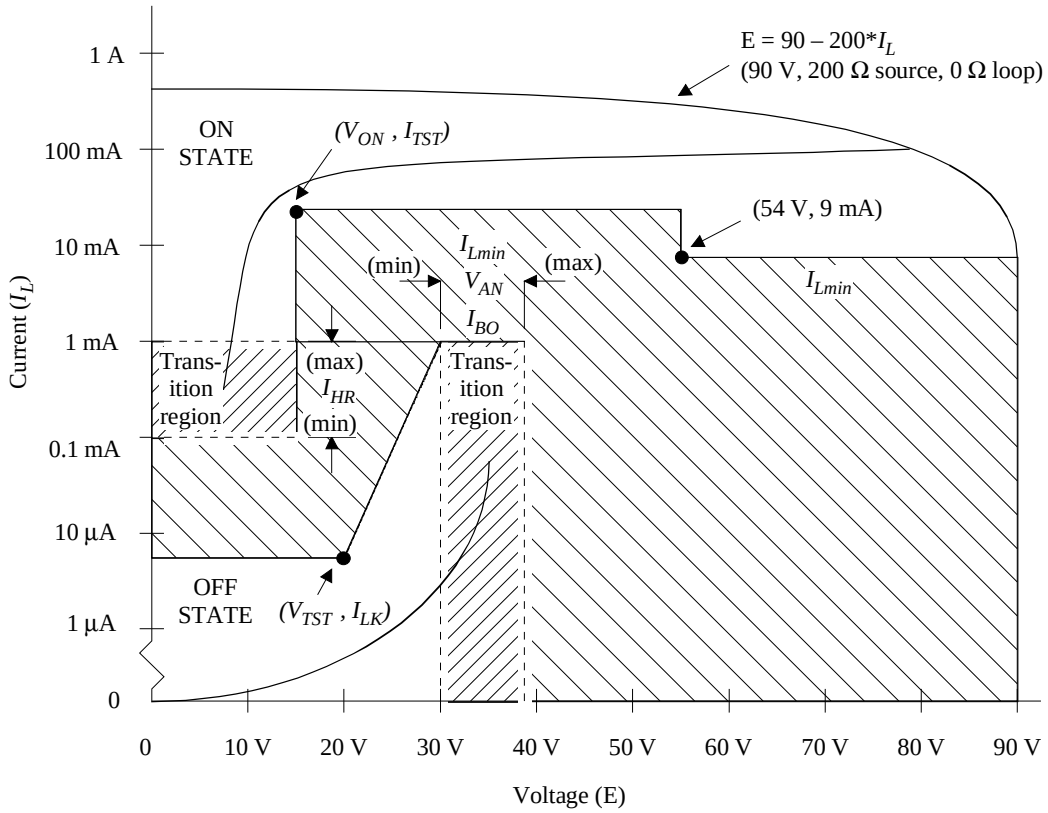
b) the STU-R may optionally limit current in excess of 25 mA (20 mA maximum sealing current + 5 mA implementation margin).

TABLE A-12

Characteristics of DC Metallic Termination at the STU-R

Type of operation	Normally OFF DC termination. Turned ON by application of metallic voltage. Held ON by loop current flow. Turned OFF by cessation of loop current flow.
Current in the ON state and at 15 V	≥ 20 mA
DC voltage drop (when ON) at 20 mA current	≤ 15 V
DC current with application of 90 V through 4 000 Ω for up to 2 s.	min 9 mA[3]. See Figure A-14.
DC leakage current (when OFF) at 20 V	≤ 5.0 μA
Activate/non-activate voltage	30.0 V DC ≤ V_{AN} ≤ 39.0 V DC
Activate (break over) current at V_{AN}	≤ 1.0 mA
Activate time for voltage ≥ V_{AN}	3 ms to 50 ms
Hold/release current	0.1 mA ≤ I_{HR} ≤ 1.0 mA
Release/non-release time for current ≤ I_{HR}	3 ms to 100 ms

[3] This requirement is intended to ensure a termination consistent with test system operation.



DC Characteristics (EITHER POLARITY)

Parameter	Meaning	Limit	Condition	Meaning
I_{LK}	Leakage current	$I_{LT} \leq 5$ µA	V_{TST} = *20 V*	Test voltage
V_{AN}	Activate/Non-activate voltage	30 V $\leq V_{AN} \leq$ 39 V		
I_{BO}	Break over current	$I_{BO} \leq$ 1.0 mA		
I_{HR}	Hold/Release current	0.1 mA $\leq I_{HR} \leq$ 1.0 mA		
V_{ON}	ON voltage	$V_{ON} \leq$ 15 V	I_{TST} = *20 mA*	Test current
I_{Lmin}	Minimum ON current	9 mA	54 V	

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FIGURE A-14

Illustration of DC Characteristics of the STU-R (Bilateral Switch and Holding Current)

A.5.4 Longitudinal Balance

For devices supporting Annex A functionality, longitudinal balance shall be specified based on the methodology of § 11.1 and the limitations of Figure 11-2. The following definitions shall be applied to the quantities in Figure 11-2.

$$LB_{\mathrm{MIN}} = 40\mathrm{dB}$$

$$f_1 = 20\mathrm{kHz}$$

$$f_2 = f_{\mathrm{sym}}/2$$

where f_{sym} is the symbol rate.

A.5.5 Longitudinal Output Voltage

For devices supporting Annex A functionality, longitudinal output voltage shall be specified based on the methodology of § 11.2. The measurement frequency range shall be between 20 kHz and 450 kHz.

A.5.6 PMMS Target Margin

If the optional line probe is selected during the G.994.1 session, the receiver shall use the negotiated target margin. If worst-case PMMS target margin is selected, then the receiver shall assume the disturbers of Table A-13 to determine if a particular rate can be supported. Reference crosstalk shall be computed as defined in § A.3.3 with the FEXT components in § A.3.3.9 ignored. The reference crosstalk specified in this section may not be representative of worst-case conditions in all networks. Differences between crosstalk environments may be compensated by adjusting the target margin.

TABLE A-13

Reference Disturbers Used During PMMS for Worst-Case Target Margin

Rate (kbit/s)	PSD (direction)	Reference disturber
All	symmetric (US/DS)	49 SHDSL
768/776	asymmetric (US)	49 HDSL
768/776	asymmetric (DS)	24 T1+24 HDSL
1 536/1 544	asymmetric (US)	39 SHDSL (NEXT only)
1 536/1 544	asymmetric (DS)	24 T1+24 SHDSL (NEXT only)

ANNEX B

Regional Requirements - Region 2

B.1 Scope

This annex describes those specifications that are unique to SHDSL systems operating under conditions such as those typically encountered within European networks. The clauses in this annex provide the additions and modifications to the corresponding clauses in the main body.

B.2 Test Loops

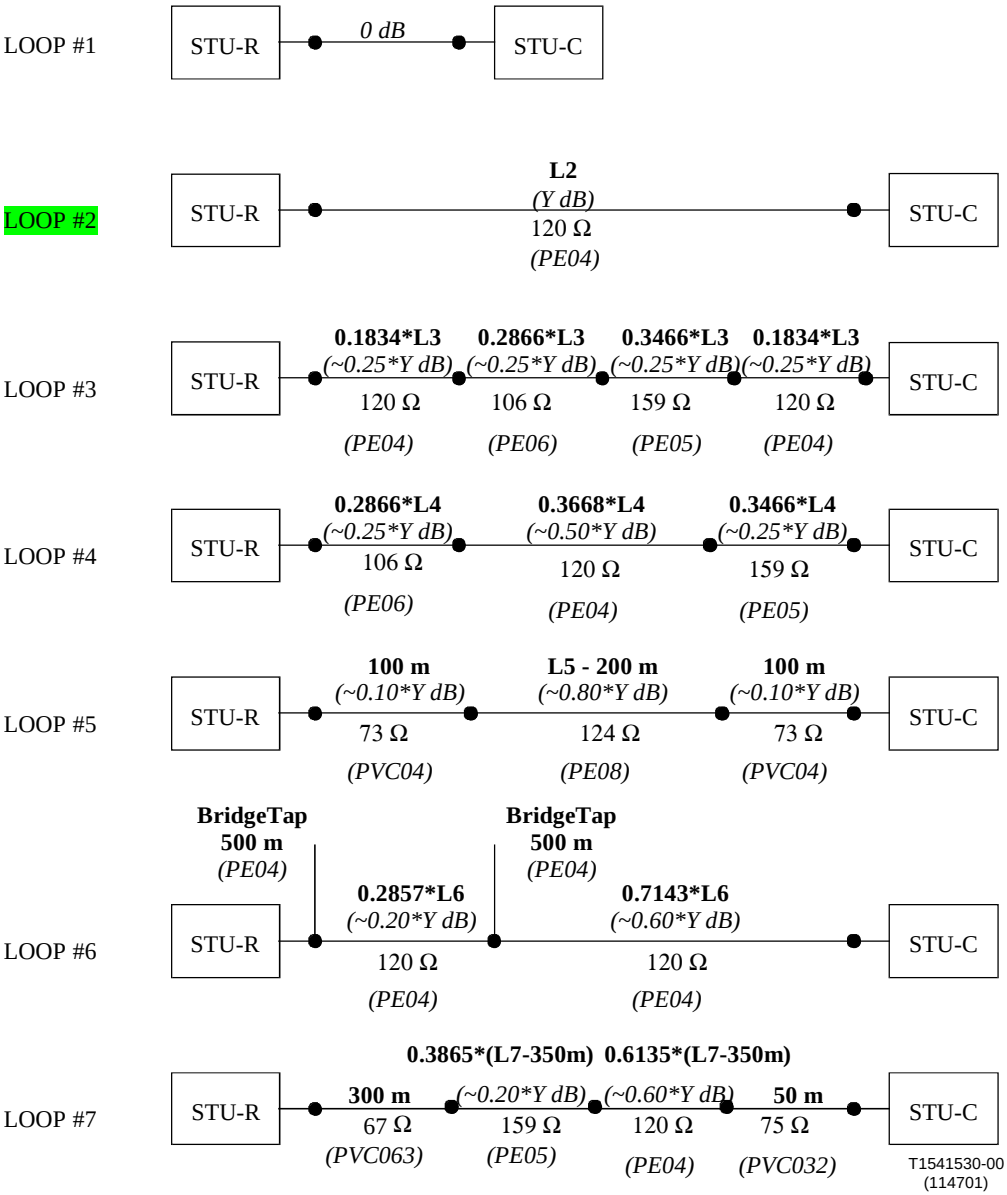
B.2.1 Functional Description

The test loops in Figure B-1 are based on the existing HDSL test loops. The length of the individual loops are chosen such that the transmission characteristics of all loops are comparable. The purpose is to stress the equalizer of the SHDSL unit under test similarly over all loops when testing SHDSL at a specific bit rate. The total length of each loop is described in terms of *physical* length, and the length of the individual sections as a fixed fraction of this total. If implementation tolerances of one test loop causes its resulting *electrical* length to be out of specification, then its total physical length shall be scaled accordingly to correct this error. One test loop includes bridged taps to achieve rapid variations in amplitude and phase characteristics of the cable transfer function. In some access networks, these bridge taps have been implemented in the past, which stresses the SHDSL modem under test differently.

Loop #1 is a symbolic name for a loop with zero (or near zero) length, to prove that the SHDSL transceiver under test can handle the potentially high signal levels when two transceivers are directly interconnected.

B.2.2 Test Loop Topology

The topology of the test loops is specified in Figure B-1. The basic test cable characteristics, the transfer function of the test loops specified using these cables and the variation of input impedance of the test loops are shown in Appendix II.



NOTE 1 - The values for *Y* and *L* are to be found in Table B-1.

NOTE 2 - Due to mismatches and bridged taps the total attenuation of the test loops differs from the sum of the attenuation of the parts.

NOTE 3 - The impedances are for information only. They refer to the characteristic impedances of the test cables as defined in Appendix II measured at 300 kHz.

FIGURE B-1

Test Loop Topology

B.2.3 Test Loop Length

The length of each test loop for SHDSL transmission systems is specified in Table B-1. The specified insertion loss Y at the specified test frequency measured with a 135 Ω termination (*electrical* length) is mandatory. If implementation tolerances of one test loop causes that its resulting *electrical* length is out of specification, then its total *physical* length shall be scaled accordingly to adjust this error.

The test frequency f_T is chosen to be a typical mid-band frequency in the spectrum of long range SHDSL systems. The length is chosen to be a typical maximum value that can be handled correctly by the SHDSL transceiver under test. This value is bit rate dependent; the higher the payload bit rate, the lower is the insertion loss that can be handled in practice.

TABLE B-1

Values of the Electrical Length Y of the SDSL Noise Test Loops, When Testing SDSL at Noise Model A

Payload Bitrate [kb/s]		**f_T [kHz]**	**Y [dB] @f_T, @135 Ω**	**L1 [m]**	**L2 [m]**	**L3 [m]**	**L4 [m]**	**L5 [m]**	**L7 [m]**		**f_T [kHz]**	**Y [dB] @f_T, @135 Ω**	**L6 [m]**
384		150	43.0	< 3	4 106	5 563	5 568	11 064	4 698		115	40.5	3 165
512		150	37.0	< 3	3 535	4 787	4 789	9 387	3 996		115	35.0	2 646
768		150	29.0	< 3	2 773	3 747	3 753	7 153	3 062		275	34.5	1 904
1 024		150	25.5	< 3	2 439	3 285	3 291	6 174	2 668		275	30.0	1 547
1 280		150	22.0	< 3	2 105	2 829	2 837	5 193	2 266		275	26.0	1 284
1 536		150	19.0	< 3	1 820	2 453	2 455	4 357	1 900		250	21.5	1 052
2 048 (s)		200	17.5	< 3	1 558	2 046	2 052	3 285	1 550		250	18.5	748
2 304 (s)		200	15.5	< 3	1 381	1 815	1 820	2 789	1 331		250	16.5	583
2 048 (a)		250	21.0	< 3	1 743	2 264	2 272	3 618	1 726		250	21.0	1 001
2 304 (a)		250	18.0	< 3	1 494	1 927	1 937	2 915	1 402		250	18.0	702

NOTE - The electrical length Y (insertion loss at specified frequency f_T) is mandatory, the (estimated) physical lengths L1-L7 are informative.
(s) those electrical lengths apply to the symmetric PSD
(a) those electrical lengths apply to the asymmetric PSD

TABLE B-2

Values of the Electrical Length Y of the SDSL Noise Test Loops, When Testing SDSL at Noise Model B, C, or D

Payload Bitrate [kb/s]		f_T [kHz]	Y [dB] @f_T, @135 Ω	L1 [m]	L2 [m]	L3 [m]	L4 [m]	L5 [m]	L7 [m]		f_T [kHz]	Y [dB] @f_T, @135 Ω	L6 [m]
384		150	50.0	< 3	4 773	6 471	6 477	13 021	5 508		115	47.5	3 859
512		150	44.0	< 3	4 202	5 692	5 698	11 344	4 814		115	41.5	3 261
768		150	35.5	< 3	3 392	4 592	4 596	8 970	3 815		275	42.0	2 536
1 024		150	32.0	< 3	3 058	4 135	4 141	7 990	3 403		275	38.0	2 223
1 280		150	28.5	< 3	2 725	3 678	3 684	7 011	3 006		275	33.5	1 816
1 536		150	25.5	< 3	2 439	3 285	3 291	6 174	2 673		250	29.0	1 680
2 048 (s)		200	24.0	< 3	2 135	2 812	2 820	4 886	2 271		250	25.5	1 426
2 304 (s)		200	21.5	< 3	1 913	2 509	2 518	4 257	2 010		250	23.0	1 208
2 048 (a)		250	28.0	< 3	2 323	3 030	3 034	5 189	2 389		250	28.0	1 607
2 304 (a)		250	25.0	< 3	2 075	2 699	2 705	4 514	2 102		250	25.0	1 387

NOTE - The electrical length Y (insertion loss at specified frequency f_T) is mandatory, the (estimated) physical lengths L1-L7 are informative.
(s) those electrical lengths apply to the symmetric PSD
(a) those electrical lengths apply to the asymmetric PSD

B.3 Performance Testing

The purpose of transmission performance tests is to stress SHDSL transceivers in a way that is representative to a high penetration of systems scenario in operational access networks. This high penetration approach enables operators to define deployment rules that apply to most operational situations. It means also that in individual operational cases, characterized by lower noise levels and/or insertion loss values, the SHDSL system under test may perform better than tested.

The design impedance R_V is 135 Ω. All spectra are representing single sided power spectral densities (PSD).

B.3.1 Test Procedure

The purpose of this section is to provide an unambiguous specification of the test set-up, the insertion path and the way signal and noise levels are defined. The tests are focused on the noise margin, with respect to the crosstalk noise or impulse noise levels when SHDSL signals under test are attenuated by standard test-loops and interfered with standard crosstalk noise or impulse noise. This noise margin indicates what increase of crosstalk noise or impulse noise level is allowed under specific operational conditions to ensure sufficient transmission quality.

B.3.2 Test Set-up Definition

Figure B-2 illustrates the functional description of the test set-up. It includes:

- A bit error ratio test set (BERTS) applies a 215 - 1 pseudo random bit sequence (PRBS) test signal to the transmitter in the direction under test at the bit rate required. The transmitter in

the opposing direction shall be fed with a similar PRBS signal, although the reconstructed signal in this path need not be monitored.

- The test loops, as specified in § B.2.
- An adding element to add the (common mode and differential mode) impairment noise (a mix of random, impulsive and harmonic noise), as specified in § B.3.5.
- An impairment generator, as specified in § B.3.5, to generate both the differential mode and common mode impairment noise, that are fed to the adding element.
- A high impedance, and well balanced differential voltage probe (e.g. better than 60 dB across the whole band of the SHDSL system under test) connected with level detectors such as a spectrum analyser or a true RMS voltmeter.
- A high impedance, and well balanced common mode voltage probe (e.g. better than 60 dB across the whole band of the SHDSL system under test) connected with level detectors such as a spectrum analyser or a true RMS voltmeter.

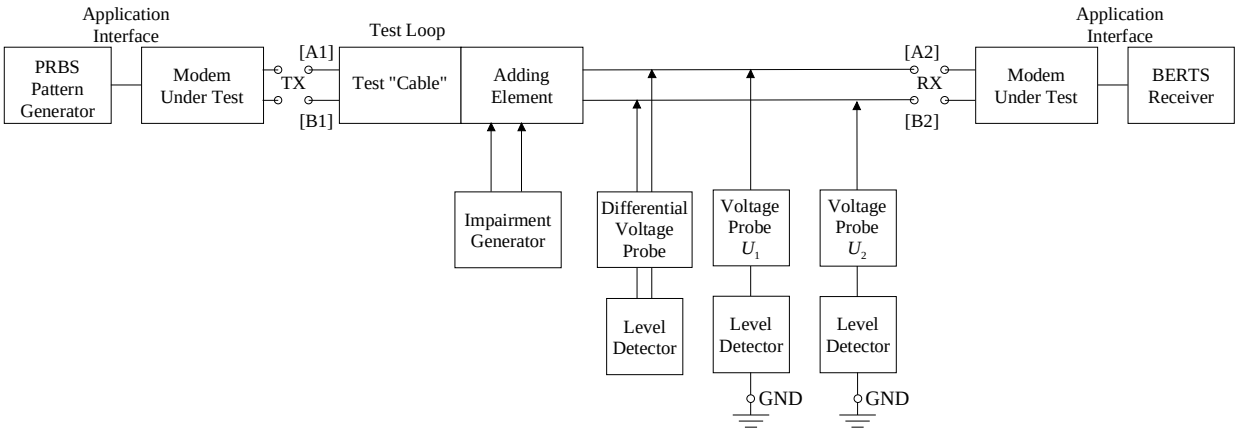


FIGURE B-2

Functional Description of the Set-up of the Performance Tests

The two-port characteristics (transfer function, impedance) of the test-loop, as specified in § B.2, are defined between port TX (node pairs A1, B1) and port RX (node pair A2, B2). The consequence is that the two-port characteristics of the test "cable" in Figure B-2 must be properly adjusted to take full account of non-zero insertion loss and non-infinite shunt impedance of the adding element and impairment generator. This is to ensure that the insertion of the generated impairment signals does not appreciably load the line.

The balance about earth, observed at port TX, at port RX, and at the tips of the voltage probe shall exhibit a value that is 10 dB greater than the transceiver under test. This is to ensure that the impairment generator and monitor function do not appreciably deteriorate the balance about earth of the transceiver under test.

The signal flow through the test set-up is from port TX to port RX, which means that measuring upstream and downstream performance requires an interchange of transceiver position and test "cable" ends.

The received signal level at port RX is the level, measured between node A2 and B2, when port TX as well as port RX are terminated with the SHDSL transceivers under test. The impairment generator is switched off during this measurement.

Test Loop #1, as specified in § B.2, shall always be used for calibrating and verifying the correct settings of generators G1-G7, as specified in § B.3.5, when performing performance tests.

The transmitted signal level at port TX is the level, measured between node A1 and B1, under the same conditions.

The impairment noise shall be a mix of random, impulsive and harmonic noise, as defined in § B.3.5. The level that is specified in § 0 is the level at port RX, measured between node A2 and B2 (and includes both differential mode and common mode impairments), while port TX as well as port RX are terminated with the design impedance R_V. These impedances shall be passive when the transceiver impedance in the switched-off mode is different from this value.

B.3.3 Signal and Noise Level Definitions

The differential mode signal and noise levels are probed with a well balanced differential voltage probe (U_1-U_2), and the differential impedance between the tips of that probe shall be higher than the shunt impedance of 100 kΩ in parallel with 10 pF. Figure B-2 shows the probe position when measuring the RX signal level at the STU-C or STU-R receiver. Measuring the TX signal level requires the connection of the tips to node pair [A1, B1].

The common mode signal and noise levels are probed with a well balanced common mode voltage probe as the voltage between nodes A2, B2, and ground. Figure 10-1 shows the position of the two voltage probes when measuring the common mode signal. The common mode voltage is defined as $(U_1 + U_2)/2$.

NOTE - The various levels (or spectral masks) of signal and noise that are specified in this document are defined at the TX or RX side of this set-up. The various levels are defined while the set-up is terminated, as described above, with design impedance R_V or with SHDSL transceivers under test.

Probing an rms-voltage U_{rms} [V] in this set-up, over the full signal band, means a power level of P [dBm] that equals:

$$P = 10 \times \log_{10} (U_{rms}^2 / R_V \times 1\,000) \text{ [dBm]}$$

Probing an rms-voltage U_{rms} [V] in this set-up, within a small frequency band of Δf [Hz], means an average spectral density level of P [dBm/Hz] within that filtered band that equals:

$$P = 10 \times \log_{10} (U_{rms}^2 / R_V \times 1\,000 / \Delta f) \text{ [dBm/Hz]},$$

where the bandwidth Δf identifies the noise bandwidth of the filter, and not the –3 dB bandwidth.

B.3.4 Performance Test Procedure

The test performance of the SHDSL transceiver shall be such that the bit error ratio (BER) on the disturbed system is less than 10^{-7}, while transmitting a pseudo random bit sequence. The BER should be measured after at least 10^9 bits have been transmitted.

The tests are carried out with a margin which indicates what increase of noise is allowed to ensure sufficient transmission quality. Network operators may calculate their own margins for planning purposes based on a knowledge of the relationship between this standard test set and their network characteristics.

A test sequence as specified in Table B-3 shall be concluded. The test loops referred to are specified in Figure B-1. The test loops are characterized by the insertion loss Y and/or the cable length L, which depend on the data rate to be transported and have to be scaled adequately.

TABLE B-3

Test Sequence for Performance Testing

N	Test Path	Direction (NOTE 6)	Comments
1	#1 (NOTE 1)	Upstream	Y = 0 dB; Test noise A (NOTES 5, 7)
2	#2	Upstream	Y = Y1 (NOTE 2); Test noise A, C and D (NOTE 7)
3	#3	Upstream	Y = Y1; Test noise D (NOTES 5, 7)
4	#4	Downstream	Y = Y1; Test noise A and C (NOTES 5, 7)
5	#5	Upstream	Y = Y1; Test noise B (NOTES 5, 7)
6	#6	Downstream	Y = Y1; Test noise A and C (NOTES 5, 7)
7	#7	Downstream	Y = Y1; Test noise A, B, C and D (NOTES 5, 7)
8			Common mode rejection test (NOTE 4)
9	(NOTE 3)	(NOTE 3)	Y = Y2; Test noise is the worst noise corresponding to the worst path of test 1 to 7. BER < 10^{-7}
10	(NOTE 3)	(NOTE 3)	Y = Y3; No added impairment; Worst path of tests 1 to 7; BER < 10^{-8}
11	#2	Upstream	Y = Y1; Impulse test as described in <TBD>
12	As <TBD>	<TBD>	Micro interruption test as described in <TBD>

NOTE 1 – Test Path = #1 means that the path under test shall be connected with test loop #1 as defined in Figure B-1.

NOTE 2 - Y1 = Y dB (as specified in Table B- for noise models B, C and D and in Table B- for noise model A), Y2 = Y1 - 10 dB, Y3 = Y1 + 3 dB.

NOTE 3 – The tests are carried out on the worst test loop from tests 1 to 7. If there are no errors, then loop #3 Upstream is taken as default.

NOTE 4 – The measuring arrangement for this test is specified in ITU-T Recommendation O.9 [13].

NOTE 5 – Only tested for lowest and highest data rate in Table B-1 or Table B-2 (that the equipment supports) and for asymmetric PSDs when supported.

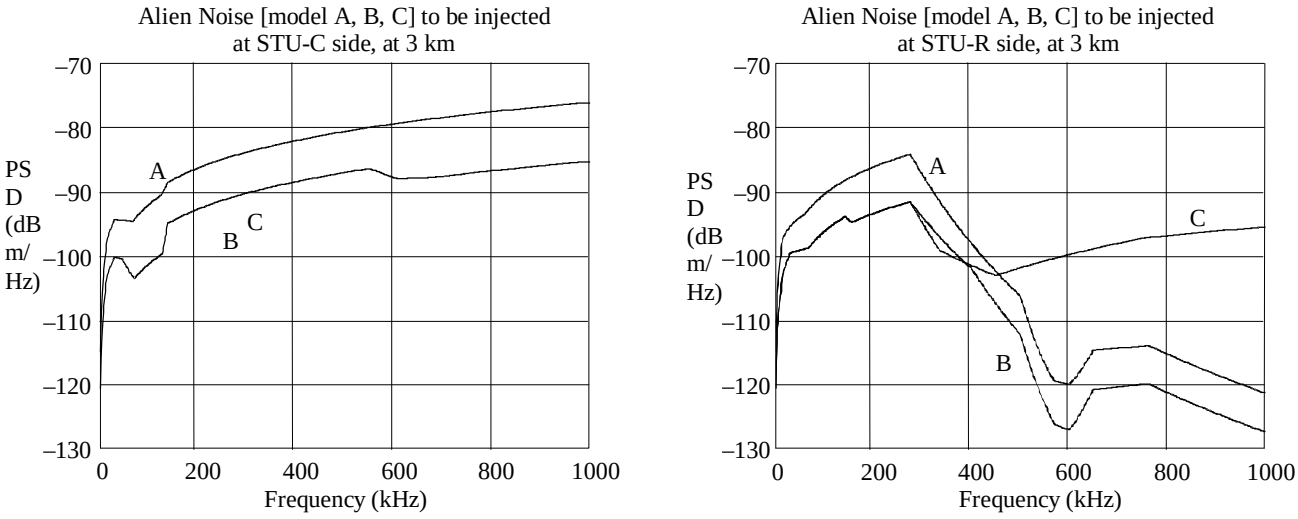
NOTE 6 – Upstream means that the unit under test is connected to the STU-C end of the test loop and downstream means that the unit under test is connected to the STU-R end of the test loop.

NOTE 7 – The BER shall be less than 10^{-7} when the test noise is increased by 6 dB (this is equivalent to 6 dB of margin).

B.3.5 Impairment Generator

The noise that the impairment generator injects into the test set-up is frequency dependent, is dependent on the length of the test loop and is also different for downstream performance tests and upstream performance tests. Figure B-3 illustrates this for the ***alien*** noise (other than the SHDSL modem under test), as described in § B.3.5.4.1, for the case that the length of test loop #1 is fixed at 3 km, using the crosstalk models described in § B.3.5.2. Figure B-4 illustrates this for various loop

lengths for the case that the ***alien*** noise of model "B" is applied. These figures are restricted to alien noise only. The self noise (of SHDSL) shall be combined with this alien noise.



NOTE - This is the noise resulting from three of the four noise models for SHDSL in the case that the length of test loop #2 is fixed at 3 km.

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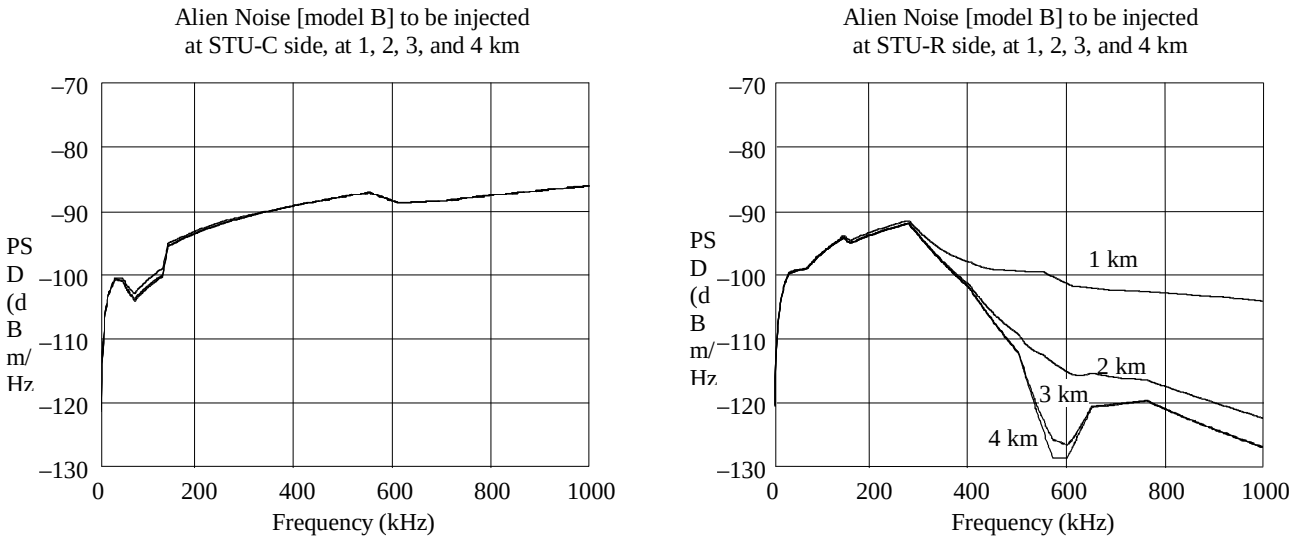
FIGURE B-3

Examples of Alien Noise Spectra that are to be Injected into the Test Set-up, While Testing SHDSL Systems



NOTE - This is the alien noise, resulting from noise model B for SHDSL, in the case that thelength of test loop #2 varies from 1 km to 4 km. This demonstrates that the test noise is length dependent, to represent the FEXT in real access network cables.

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FIGURE B-4

Examples of Alien Noise Spectra that are to be Injected into the Test Set-up, While Testing SHDSL Systems

The definition of the impairment noise for SHDSL performance tests is very complex and for the purposes of this Recommendation it has been broken down into smaller, more easily specified components. These separate, and uncorrelated, impairment "generators" may therefore be isolated and summed to form the impairment generator for the SHDSL system under test. The detailed specifications for the components of the noise model(s) are given in this section, together with a brief explanation.

B.3.5.1 Functional Description

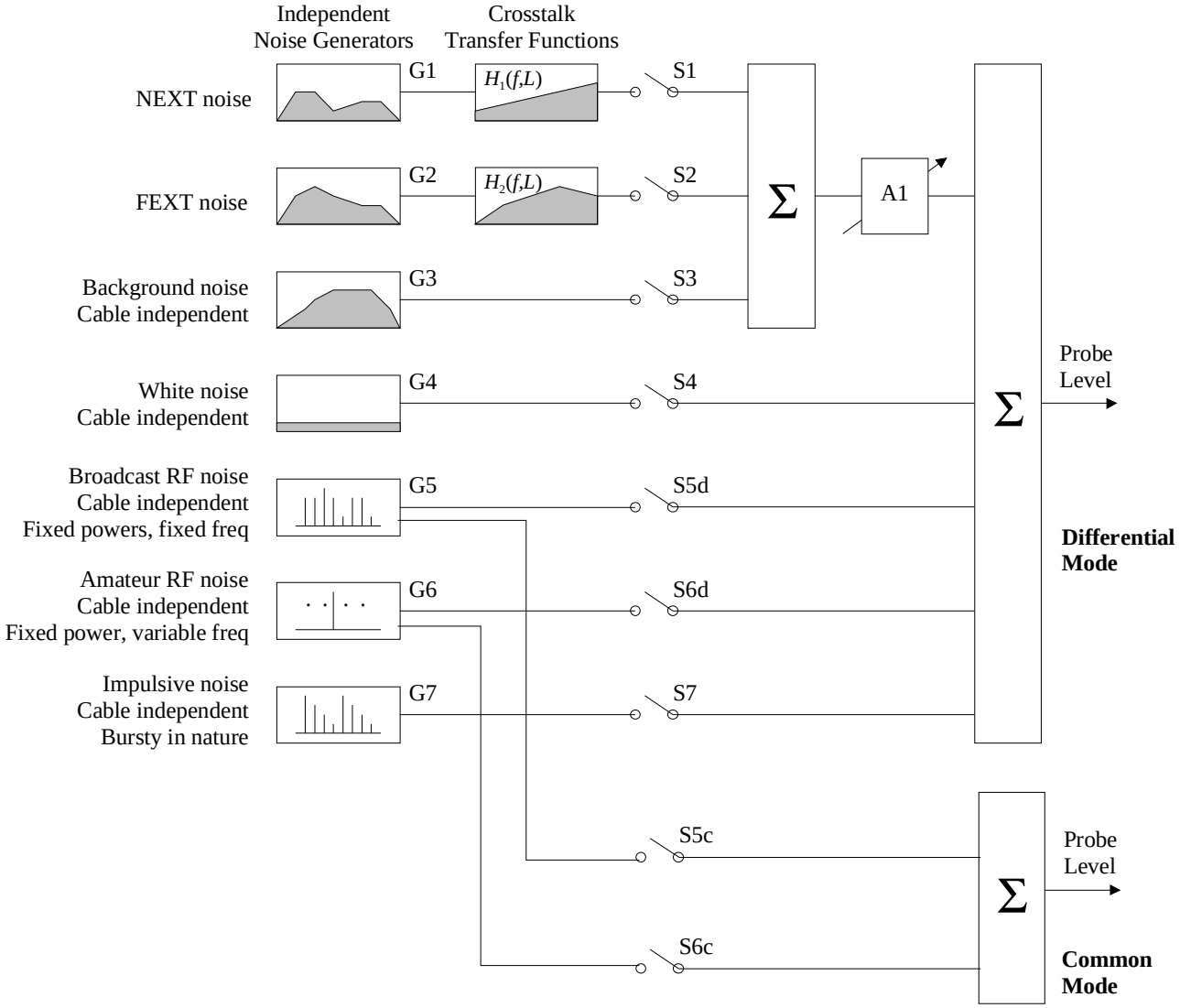
Figure B-5 defines a functional diagram of the composite impairment noise. It defines a functional description of the combined impairment noise as it must be probed at the receiver input of the SHDSL transceiver under test. The probing is described in § B.3.3.

The functional diagram has the following elements:

- The seven impairment "generators" G1 to G7 generate noise as defined in § B.3.5.3.1 to § B.3.5.3.7. Their noise characteristics are independent from the test loops and bit rates.
- The transfer function $H_1(f, L)$ models the length and frequency dependency of the NEXT impairment, as specified in § B.3.5.3.1. The transfer function is independent of the test loops, but changes with the electrical length of the test loop. Its transfer function changes with the frequency f, roughly according to $f^{0.75}$.
- The transfer function $H_2(f, L)$ models the length and frequency dependency of the FEXT impairment, as specified in § B.3.5.3.2. Its transfer function is independent of the test loops, but changes with the electrical length of the test loop. Its transfer function changes with the frequency f, roughly according to f times the cable transfer function.
- Switches S1-S7 determine whether or not a specific impairment generator contributes to the total impairment during a test.

- Amplifier A1 models the property to increase the level of some generators simultaneously to perform the noise margin tests. A value of *x* dB means a frequency independent increase of the level by *x* dB over the full band of the SHDSL system under test, from f_L to f_H. Unless otherwise specified, its gain is fixed at 0 dB.

In a practical implementation of the test set-up, there is no need to give access to any of the internal signals of the diagram in Figure B-5. These functional blocks may be incorporated with the test loop and the adding element as one integrated construction.



NOTE 1: Generator G7 is the only one that is symbolically shown in the time domain.

NOTE 2: The precise definition of impulse noise margin is for further study.

FIGURE B-5

Functional Diagram of the Composition of the Impairment Noise

This functional diagram will be used for impairment tests in downstream and upstream direction. Several scenarios have been identified to be applied to SHDSL testing. These scenarios are intended to be representative of the impairments found in metallic access networks.

Each scenario (or noise model) results in a length dependent PSD description of noise. Each noise model is subdivided into two parts: one to be injected at the STU-C side, and another to be injected at the STU-R side of the SHDSL link under test. Some of the seven individual impairment "generators" G1 to G7 are therefore defined by more than one noise model.

Each test has its own impairment specification. The overall impairment noise shall be characterized by the sum of the individual components as specified in the relevant sub-clauses. This combined impairment noise is applied to the receiver under test, at either the STU-C (for upstream) or STU-R (for downstream) ends of the test loop.

B.3.5.2 Cable Crosstalk Models

The purpose of the cable cross-talk models is to model both the length and frequency dependency of crosstalk measured in real cables. These crosstalk transfer functions adjust the level of the noise generators in Figure B-5 when the electrical length of the test loops is changed. The frequency and length dependency of these functions is in accordance with observations from real cables. The specification is based on the following constants, parameters and functions:

- Variable f identifies the frequency in Hz.
- Constant f_0 identifies a chosen reference frequency, which was set to 1 MHz.
- Variable L identifies an average physical length in meters. This physical length is calculated from the cable models in Appendix II from the specified electrical length. Values are summarized in Table B-1 for each combination of payload bit rate, noise model, and test loop.
- Constant L_0 identifies a chosen reference length, which was set to 1 km.
- Function $s_{T0}(f,L)$ represents the frequency and length dependent amplitude of the insertion loss of the actual test loop terminated into 135 Ω.
- Constant K_{xn} identifies an empirically obtained number that scales the NEXT transfer function $H_1(f, L)$. The resulting transfer function represents a power summed crosstalk model of the NEXT as it was observed in a test cable. Although several disturbers and wire pairs were used, this function $H_1(f, L)$ is scaled down as if it originates from a single disturber in a single wire pair.
- Constant K_{xf} identifies an empirically obtained number that scales the FEXT transfer function $H_2(f, L)$. The resulting transfer function represents a power summed crosstalk model of the FEXT as it was observed in a test cable. Although several disturbers and wire pairs were used, this function $H_2(f, L)$ is scaled down as if it originates from a single disturber in a single wire pair.

The transfer functions in Table B-4 shall be used as crosstalk transfer functions in the impairment generator.

TABLE B-4

Definition of the crosstalk transfer functions

$H_1(f,L) = K_{xn} \times \left(\frac{f}{f_0}\right)^{0.75} \times \sqrt{1-\left\|s_{T0}(f,L)\right\|^4}$ $H_2(f,L) = K_{xf} \times \left(\frac{f}{f_0}\right) \times \sqrt{\frac{L}{L_0}} \times \left\|s_{T0}(f,L)\right\|$
$K_{xn} = 10^{(-50/20)} \approx 0.0032, \quad f_0 = 1$ MHz $K_{xf} = 10^{(-45/20)} \approx 0.0056, \quad L_0 = 1$ km $s_{T0}(f,L)$ = test loop insertion loss

B.3.5.3 Individual Impairment Generators

B.3.5.3.1 Equivalent NEXT Disturbance Generator [G1.xx]

The NEXT noise generator represents the equivalent disturbance of all impairment that is identified as crosstalk noise from a predominantly near end origin. This noise, filtered by the NEXT crosstalk coupling function of § B.3.5.2, will represent the contribution of all NEXT to the composite impairment noise of the test.

The PSD of this noise generator is one of the PSD profiles, as specified in § B.3.5.4. For testing upstream and downstream performance, different PSD profiles shall be used, as specified below.

G1.C.# = X.C.#

G1.R.# = X.R.#

The symbols in this expression, refer to the following:

- Symbol "#" is a placeholder for noise model "A", "B" , "C" or "D".
- Symbol "X.C.#" and "X.R.#" refer to the crosstalk profiles, as defined in § B.3.5.4.

This PSD is not related to the cable because the cable portion is modelled separately as transfer function $H_1(f, L)$, as specified in § B.2.2.

The noise of this noise generator shall be uncorrelated with all the other noise sources in the impairment generator, and uncorrelated with the SHDSL system under test. The noise shall be random in nature and near Gaussian distributed, as specified in § B.3.5.4.2.

B.3.5.3.2 Equivalent FEXT Disturbance Generator [G2.xx]

The FEXT noise generator represents the equivalent disturbance of all impairment that is identified as crosstalk noise from a predominantly far end origin. This noise, filtered by the FEXT crosstalk coupling function of § B.3.5.2, will represent the contribution of all FEXT to the composite impairment noise of the test.

The PSD of this noise generator is one of the PSD profiles, as specified in § B.3.5.4.1. For testing upstream and downstream performance, different PSD profiles shall be used, as specified below.

G2.C.# = X.R.#

G2.R.# = X.C.#

The symbols in this expression, refer to the following:

- Symbol "#" is a placeholder for noise model "A", "B", "C" or "D".
- Symbol "X.C.#" and "X.R.#" refers to the crosstalk profiles, as defined in § B.3.5.4.

This PSD is not related to the cable because the cable portion is modelled separately as transfer function $H_2(f, L)$, as specified in § B.2.2.

The noise of this noise generator shall be uncorrelated with all the other noise sources in the impairment generator, and uncorrelated with the SHDSL system under test. The noise shall be random in nature and near Gaussian distributed, as specified in § B.3.5.4.2.

B.3.5.3.3 Background Noise Generator [G3]

The background noise generator is inactive and set to zero.

B.3.5.3.4 White Noise Generator [G4]

The white noise generator has a fixed, frequency independent value, and is set to −140 dBm/Hz, into 135 Ω. The output signal of this noise generator shall be uncorrelated with all the other noise sources in the impairment generator, and uncorrelated with the SHDSL system under test. The noise shall be random in nature and near Gaussian distributed, as specified in § B.3.5.4.2.

B.3.5.3.5 Broadcast RF Noise Generator [G5]

The broadcast RF noise generator represents the discrete tone-line interference caused by amplitude modulated broadcast transmissions in the Short Wave (SW), Medium Wave (MW), and Long Wave (LW) bands which ingress into the differential or transmission mode of the wire-pair. These interference sources have more temporal stability than the amateur/ham interference because their carrier is not suppressed. The modulation index (MI) is usually up to 80%. These signals are detectable using a spectrum analyser and result in line spectra of varying amplitude in the frequency band of the SHDSL system under test. Maximum observable power levels of up to TBD dBm can occur on telephone lines in the distant vicinity of broadcast AM transmitters. The noise is typically dominated by the closest 10 or so transmitters to the victim wire-pair.

Several noise models are specified in this sub-clause. The average minimum power of each carrier frequency is specified in Table B-5 for each model, but these values are for further study.

TABLE B-5

Average minimum RFI noise power versus frequency

frequency	99	207	333	387	531	603	711	801	909	981	kHz
power	–70	–40	–60	–60	–40	–50	–40	–50	–60	–60	dBm

B.3.5.3.6 Amateur RF Noise Generator [G6]

The amateur radio noise generator is identical to the broadcast RF noise generator with different frequency and power values. These values are for further study.

B.3.5.3.7 Impulse Noise Generator [G7]

A test with this noise generator is required to prove the burst noise immunity of the SHDSL transceiver. This immunity shall be demonstrated on short and long loops and noise to model crosstalk and RFI.

B.3.5.4 Profiles of the Individual Impairment Generators

Crosstalk noise represents all impairment that originates from systems connected to adjacent wire pairs that are bundled in the same cable. Their wires are coupled to the wires of the xDSL system under test, causing this spectrum of crosstalk noise to vary with the electrical length of the test loop.

To simplify matters, the definition of crosstalk noise has been broken down into smaller, more easily specified components. The two generators G1 and G2 represent the "equivalent disturbance". Their noise level originate from a mixture of many disturbers in a real scenario, as if all disturbers are collocated at the ends of the test loops.

This equivalent disturbance, filtered by the NEXT and FEXT coupling functions, will represent the crosstalk noise that is to be injected in the test set up. This approach has isolated their definition from the NEXT and FEXT coupling functions of the cable. The noise generated by these two equivalent disturbers is specified in this section in the frequency domain as well as in the time domain.

The frequency domain characteristics of each generator G1 and G2 is defined by a spectral profile, so each noise model has its own pair of spectral profiles.

- The profiles X.C.# in this section describe the total equivalent disturbance of a technology mix that is virtually co-located at the STU-C end of the test loop. This noise is represented by equivalent disturbance generator G1, when stressing upstream signals, and by equivalent disturbance generator G2 when stressing downstream signals.
- The profiles X.R.# in this section describe the total equivalent disturbance of a technology mix that is virtually co-located at the STU-R end of the test loop. This noise is represented by equivalent disturbance generator G2, when stressing upstream signals, and by equivalent disturbance generator G1 when stressing downstream signals.

Note that the PSD levels of equivalent disturbance generator G1 and G2 are interchanged when changing from upstream testing to downstream testing.

B.3.5.4.1 Frequency Domain Profiles for SHDSL

This sub-clause specifies the PSD profiles X.R.# and X.C.# that apply for the equivalent disturbers G1 and G2 when testing SHDSL systems. In this nomenclature is "#" used as a placeholder for noise model "A", "B" ,"C" and "D".

Four noise models have been defined for SHDSL:

- **Type "A" models** are intended to represent a high penetration scenario where the SHDSL system under test is placed in a distribution cable (up to hundreds of wire pairs) that is filled with many other (potentially incompatible) transmission systems.
- **Type "B" models** are intended to represent a medium penetration scenario where the SHDSL system under test is placed in a distribution cable (up to tens of wire pairs) that is filled with many other (potentially incompatible) transmission systems.
- **Type "C" models** are intended to represent a legacy scenario that accounts for systems such as ISDN-PRI (HDB3), in addition to the medium penetration scenario of model "B".
- **Type "D" models** are intended as reference scenario to demonstrate the difference between a cable filled with SHDSL only, or filled with a mixture of SHDSL techniques.

The PSD profiles for each noise model are build up by a weighed sum of two individually defined profiles: self and alien crosstalk profiles.

$$X.C.\# = (XS.C.\# \blacklozenge XA.C.\#)$$

$$X.R.\# = (XS.R.\# \blacklozenge XA.R.\#)$$

The symbols in this expression, refer to the following:

- Symbol "#" is used as a placeholder for noise model "A", "B", "C" or "D".
- Symbol "XS.C.#" and "XS.R.#" refers to the self crosstalk profiles, as defined in B.3.5.4.1.1.
- Symbol "XA.C.#" and "XA.R.#" refers to the alien crosstalk profiles, as defined in B.2.5.4.1.2.
- Symbol "♦" refers to the crosstalk sum of two PSDs, defined as $P_X = \left(P_{XS}{}^{K_n} + P_{XA}{}^{K_n}\right)^{1/K_n}$, where P denotes the PSDs in W/Hz, and K_n = 1/0.6.

These profiles shall be met for all frequencies between 1 kHz to 1 MHz.

B.3.5.4.1.1 Self Crosstalk Profiles

The noise profiles XS.C.# and XS.R.#, representing the equivalent disturbance of self crosstalk, are implementation specific of the SHDSL system under test. Transceiver manufacturers are left to determine these levels. For compliance with the requirements of this recommendation, the transceiver manufacturer shall determine the signal spectrum of the SHDSL system under test, as it can be observed at the TX port of the test set-up as described in § B.3.2. The measurement bandwidth for PSD shall be 1 kHz or less.

For testing SHDSL, four noise models for self crosstalk have been defined. The STU-R and STU-C profiles are specified in Table B-6.

In this nomenclature is "#" a placeholder for model "A", "B" ,"C" or "D". "SHDSL.dn" is the signal spectrum that SHDSL transmits in downstream direction, and "SHDSL.up" in upstream direction.

TABLE B-6

Definition of the Self Crosstalk for SHDSL Testing

	Model A (XS.#.A)	**Model B (XS.#.B)**	**Model C (XS.#.C)**	**Model D (XS.#.D)**
XS.C.#:	"SHDSL.dn" + 11.7 dB	"SHDSL.dn" + 7.1 dB	"SHDSL.dn" + 7.1 dB	"SHDSL.dn" + 10.1 dB
XS.R.#:	"SHDSL.up" + 11.7 dB	"SHDSL.up" + 7.1 dB	"SHDSL.up" + 7.1 dB	"SHDSL.up" + 10.1 dB
NOTE - The different noise models use different Gain factors.				

B.3.5.4.1.2 Alien Crosstalk Profiles

The noise profiles XA.C.# and XA.R.#, representing the equivalent disturbance of alien crosstalk, are implementation specific of the SHDSL system under test. For testing SHDSL, four noise models for alien crosstalk have been defined. The STU-C profiles are specified in Table B-7 and the STU-R profiles in Table B-8. Each PSD profile originates from a mix of disturbers. The alien noise in model D is made inactive, to achieve one pure self crosstalk scenario.

TABLE B-7

Break Frequencies of the "XA.C.#" PSD Profiles that Specify the Equivalent Disturbance Spectra of Alien Disturbers

XA.C.A [Hz]	***135 Ω*** **[dBm/Hz]**	**XA.C.B [Hz]**	***135 Ω*** **[dBm/Hz]**	**XA.C.C [Hz]**	***135 Ω*** **[dBm/Hz]**	**XA.C.D [Hz]**	***135 Ω*** **[dBm/Hz]**
1	–20.0	1	–25.7	1	–25.7		
15 k	–20.0	15 k	–25.7	15 k	–25.7		
30 k	–21.5	30 k	–27.4	30 k	–27.4	*ALL*	-∞
67 k	–27.0	45 k	–30.3	45 k	–30.3		
125 k	–27.0	70 k	–36.3	70 k	–36.3		
138 k	–25.7	127 k	–36.3	127 k	–36.3		
400 k	–26.1	138 k	–32.1	138 k	–32.1		
1104 k	–26.1	400 k	–32.5	400 k	–32.5		
2.5 M	–66.2	550 k	–32.5	550 k	–32.5		
4.55 M	–96.5	610 k	–34.8	610 k	–34.8		
30 M	–96.5	700 k	–35.4	700 k	–35.3		
		1 104 k	–35.4	1 104 k	–35.3		
		4.55 M	–03.0	1.85 M	–58.5		
		30 M	–103.0	22.4 M	–103.0		
				30 M	–103.0		

NOTE - The PSD profiles are constructed with straight lines between these break frequencies, when plotted against a ***logarithmic*** frequency scale and a ***linear*** dBm scale. The levels are defined with into a 135 Ω resistive load.

TABLE B-8

Break Frequencies of the "XA.R.#" PSD Profiles that Specify the Equivalent Disturbance Spectra of Alien Disturbers

XA.R.A [Hz]	***135 Ω*** **[dBm/Hz]**	**XA.R.B [Hz]**	***135 Ω*** **[dBm/Hz]**	**XA.R.C [Hz]**	***135 Ω*** **[dBm/Hz]**	**XA.R.D [Hz]**	***135 Ω*** **[dBm/Hz]**
1	–20.0	1	–25.7	1	–25.7		
15 k	–20.0	15 k	–25.7	15 k	–25.7		
60 k	–25.2	30 k	–26.8	30 k	–26.8	*ALL*	-∞
276 k	–25.8	67 k	–31.2	67 k	–31.2		
500 k	–51.9	142 k	–31.2	142 k	–31.2		
570 k	–69.5	156 k	–32.7	156 k	–32.7		
600 k	–69.9	276 k	–33.2	276 k	–33.2		
650 k	–62.4	400 k	–46.0	335 k	–42.0		
763 k	–62.4	500 k	–57.9	450 k	–47.9		
1.0 M	–71.5	570 k	–75.7	750 k	–45.4		
2.75 M	–96.5	600 k	–76.0	1040 k	–45.5		
30 M	–96.5	650 k	–68.3	2.46 M	–63.6		
		763 k	–68.3	23.44 M	–103.0		
		1.0 M	–77.5	30 M	–103.0		
		2.8 M	–103.0				
		30 M	–103.0				

NOTE - The PSD profiles are constructed with straight lines between these break frequencies, when plotted against a ***logarithmic*** frequency scale and a ***linear*** dBm scale. The levels are defined with into a 135 Ω resistive load.

B.3.5.4.2 Time Domain Profiles of Generators G1-G4

The noise, as specified in the frequency domain in § B.3.5.3.1 to § B.3.5.3.4, shall be random in nature and near Gaussian distributed. This means that the amplitude distribution function of the combined impairment noise injected at the adding element shall lie between the two boundaries as illustrated in Figure B-6, where the non-shaded area is the allowed region. The boundaries of the mask are specified in Figure B-9.

The amplitude distribution function $F(a)$ of noise $u(t)$ is the fraction of the time that the absolute value of $u(t)$ exceeds the value "a". From this definition, it can be concluded that $F(0) = 1$ and that $F(a)$ monotonically decreases up to the point where "a" equals the peak value of the signal. From there on, $F(a)$ vanishes:

$$F(a) = 0 \text{, for } a \geq \left| u_{peak} \right| .$$

The boundaries on the amplitude distribution ensure that the noise is characterized by peak values that are occasionally significantly higher than the rms-value of that noise (up to 5 times the rms-value).

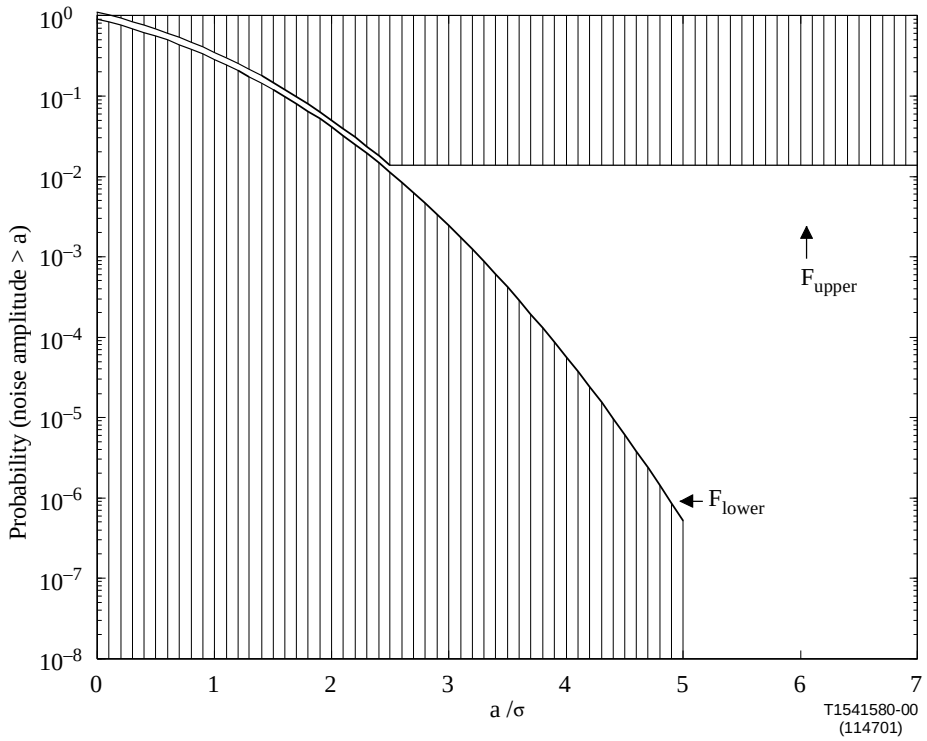


FIGURE B-6

Mask for the Amplitude Distribution Function

TABLE B-9

Upper and Lower Boundaries of the Amplitude Distribution Function of the Noise

Boundary (σ = rms value of noise)	Interval
$F_{lower}(a) = (1 - \varepsilon) \cdot \{1 - erf((a/\sigma)/\sqrt{2}) \}$	$0 \le a/\sigma < CF$
$F_{lower}(a) = 0$	$CF \le a/\sigma < \infty$
$F_{upper}(a) = (1 + \varepsilon) \cdot \{1 - erf((a/\sigma)/\sqrt{2}) \}$	$0 \le a/\sigma < A$
$F_{upper}(a) = (1 + \varepsilon) \cdot \{1 - erf(A/\sqrt{2}) \}$	$A \le a/\sigma < \infty$

Parameter	Value
crest factor	CF = 5
Gaussian gap	ε = 0.1
	A = CF/2 = 2.5

The meaning of the parameters in Table B-3 is as follows:

– CF denotes the minimum crest factor of the noise, that characterizes the ratio between the absolute peak value and rms value (CF= $|u_{peak}| / u_{rms}$).

– ε denotes the Gaussian gap that indicates how "close" near Gaussian noise approximates true Gaussian noise.

– A denotes the point beyond which the upper limit is alleviated to allow the use of noise signals of practical repetition length.

B.3.5.5 Measurement of Noise Margin

At start-up, the level and shape of crosstalk noise or impulse noise are adjusted, while their level is probed at port RX to meet the impairment level specification in § B.3.4. This relative level is referred to as 0 dB. The transceiver link is subsequently activated, and the bit error ratio of the link is monitored.

B.3.5.6 Measurement of Crosstalk Noise Margin

For measuring the crosstalk margin, the crosstalk noise level of the impairment generator as defined in Table B-7 or Table B-8 shall be increased by adjusting the gain of amplifier A1 in Figure B-2, equally over the full frequency band of the SHDSL system under test, until the bit error ratio is higher than 10^{-7}. This BER will be achieved at an increase of noise of x dB, with a small uncertainty of Δx dB. This value x is defined as the crosstalk noise margin with respect to a standard noise model.

The noise margins shall be measured for upstream as well as downstream transmission.

B.3.5.7 Measurement of Impulse Noise Margin

For further study.

B.4 PSD Masks

For all data rates, the measured transmit PSD of each STU shall not exceed the PSD masks specified in this section ($PSDMASK_{SHDSL}(f)$), and the measured total power into 135 Ω shall fall within the range specified in this section ($P_{SHDSL} \pm 0.5$ dB).

Support for the symmetric PSDs specified in § B.4.1 shall be mandatory for all supported data rates. Support for the asymmetric PSDs specified in § B.4.2 shall be optional.

Table B-10 lists the supported PSDs and the associated constellation sizes.

TABLE B-10

PSD and constellation size

Symmetric PSDs		**Asymmetric PSDs**			
DS	US	DS	US	DS	US
16-TCPAM	16-TCPAM	16-TCPAM	16-TCPAM	8-TCPAM	16-TCPAM
Mandatory		Optional		For further study	

For the 16-TCPAM upstream and downstream constellations shown in Table B-10, the details of payload data rate, the associated symbol rate, and the mapping of bits per symbol are specified in Table B-11.

TABLE B-11

Framed Data Mode Rates

Payload Data Rate, *R* (kbit/s)	**Modulation**	**Symbol Rate (ksymbol/s)**	***K* (Bits per Symbol)**
$R=n\times64+(i)\times8$	16-TCPAM	$(R+8)\div3$	3

As specified in § 5, the allowed rates are given by $n \times 64 + i \times 8$ kbit/s, where $3 \le n \le 36$ and $0 \le i \le 7$. For $n = 36$, i is restricted to the values of 0 or 1.

B.4.1 Symmetric PSD Masks

For all values of framed data rate available in the STU, the following set of PSD masks ($PSDMASK_{\mathrm{SHDSL}}(f)$) shall be selectable:

$$PSDMASK_{SHDSL}(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \frac{K_{SHDSL}}{135} \times \frac{1}{f_{sym}} \times \frac{\left[\sin\left(\frac{\pi f}{Nf_{sym}}\right)\right]^2}{\left(\frac{\pi f}{Nf_{sym}}\right)^2} \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^{2\times Order}} \times 10^{\frac{MaskedOffsetdB(f)}{10}}, & f < f_{\mathrm{int}} \\ 0.5683\times10^{-4}\times f^{-1.5}, \quad f_{\mathrm{int}} \le f \le 1.5\text{MHz} \\ -90\ \text{dBm/Hz peak with maximum power in a } [f, f+1\text{MHz}] \text{ window of } -50\ \text{dBm}, \\ \qquad 1.5\text{MHz} < f \le 11.04\text{MHz} \end{cases}$$

where *MaskOffsetdB*(*f*) is defined as:

$$MaskOffsetdB(f) = \begin{cases} 1+0.4\times\frac{f_{3dB}-f}{f_{3dB}}, & f < f_{3dB} \\ 1, & f \ge f_{3dB} \end{cases}$$

The inband PSD for $0 < f < 1.5$ MHz shall be measured with a 10 kHz resolution bandwidth.

f_{int} is the frequency where the two functions governing $PSDMASK_{\mathrm{SHDSL}}(f)$ intersect in the frequency range from 0 to Nf_{sym}. PBO is the power backoff value in dB. K_{SHDSL}, *Order*, *N*, f_{sym}, $f_{3\ \mathrm{dB}}$, and P_{SHDSL} are defined in Table B-12. P_{SHDSL} is the range of power in the transmit PSD with 0 dB power backoff. *R* is the payload data rate.

TABLE B-12

Symmetric PSD parameters

Payload Data Rate, *R* (kbit/s)	K_{SHDSL}	***Order***	***N***	**Symbol Rate f_{sym} (ksymbol/s)**	$F_{3\ \mathrm{dB}}$	P_{SHDSL} **(dBm)**
$R < 2\ 048$	7.86	6	1	$(R+8)/3$	$1.0 \times f_{\mathrm{sym}}/2$	$P1(R) \le P_{\mathrm{SHDSL}} \le 13.5$
$R \ge 2\ 048$	9.90	6	1	$(R+8)/3$	$1.0 \times f_{\mathrm{sym}}/2$	14.5

$P1(R)$ is defined as follows:

$$P1(R) = 0.3486 \log_2 (R \times 1000 + 8000) + 6.06 \text{ dBm}$$

For 0 dB power backoff, the measured transmit power into 135 Ω shall fall within the range $P_{SHDSL} \pm 0.5$ dB. For power backoff values other than 0 dB, the measured transmit power into 135 Ω shall fall within the range $P_{SHDSL} \pm 0.5$ dB minus the power backoff value in dB. The measured transmit PSD into 135 Ω shall remain below $PSDMASK_{SHDSL}(f)$.

Figure B-7 shows the PSD masks with 0 dB power backoff for payload data rates of 256, 512, 768, 1 536, 2 048, and 2 304 kbit/s.

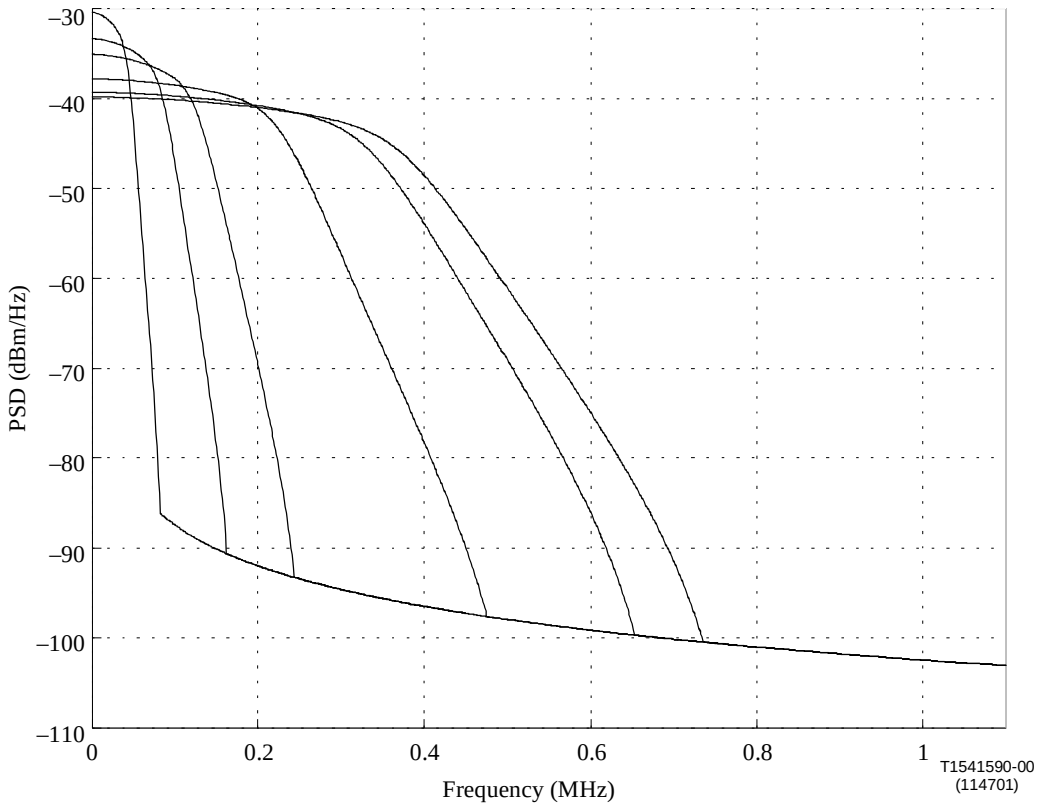


FIGURE B-7

PSD Masks for 0 dB Power Backoff

The equation for the nominal PSD measured at the terminals is:

$$NominalPSD(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \frac{K_{SHDSL}}{135} \times \frac{1}{f_{sym}} \times \frac{\left[\sin\left(\frac{\pi f}{N f_{sym}}\right)\right]^2}{\left(\frac{\pi f}{N f_{sym}}\right)^2} \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^{2\times Order}} \times \frac{f^2}{f^2 + f_c^2}, & f < f_{\text{int}} \\ 0.5683\times 10^{-4} \times f^{-1.5}, \quad f_{\text{int}} \le f \le 1.5\text{MHz} & \\ -90\ \text{dBm/Hz peak with maximum power in a}\ [f,\ f+1\text{MHz}]\ \text{window of}\ -50\ \text{dBm}, & \\ \qquad 1.5\text{MHz} < f \le 11.04\text{MHz} & \end{cases}$$

where f_c is the transformer cutoff frequency, assumed to be 5 kHz. Figure B-8 shows the nominal transmit PSDs with 13.5 dBm power for payload data rates of 256, 512, 768, 1 536, 2 048, and 2 304 kbit/s. NOTE - The nominal PSD is given for information only.

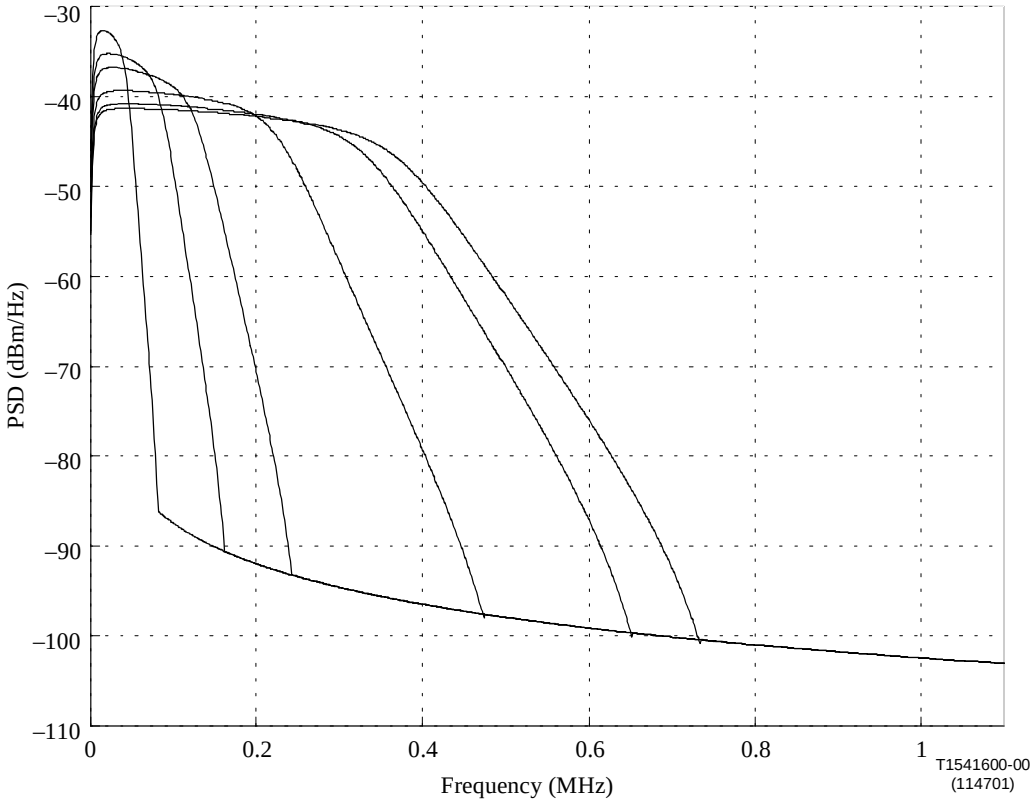


FIGURE B-8

Nominal Symmetric PSDs for 0 dB Power Backoff

NOTE: In this section, *PSDMASK(f)* and *NominalPSD(f)* are in units of W/Hz unless otherwise specified, and *f* is in units of Hz.

B.4.2 Asymmetric 2.048 Mbit/s and 2.304 Mbit/s PSD Masks

The asymmetric PSD mask set specified in this section shall optionally be supported for the 2.048 Mbit/s and the 2.304 Mbit/s payload data rate. Power and power spectral density is measured into a load impedance of 135 Ω.

For the 2.048 Mbit/s and the 2.304 Mbit/s payload data rates available in the STU, the following set of PSD masks ($PSDMASK_{SHDSL}(f)$) shall be selectable:

$$PSDMASK_{SHDSL}(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \frac{K_{SHDSL}}{135} \times \frac{1}{f_x} \times \frac{\left[\sin\left(\frac{\pi f}{f_x}\right)\right]^2}{\left(\frac{\pi f}{f_x}\right)^2} \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^{2\times Order}} \times 10^{\frac{MaskedOffsetdB(f)}{10}}, & f < f_{\text{int}} \\ 0.5683 \times 10^{-4} \times f^{-1.5}, & f_{\text{int}} \le f \le 1.5\text{MHz} \\ -90 \text{ dBm/Hz peak with maximum power in a } [f,\ f+1\text{MHz}] \text{ window of } -50 \text{ dBm}, & 1.5\text{MHz} < f \le 11.04\text{MHz} \end{cases}$$

where *MaskOffsetdB*(*f*) is defined as:

$$MaskOffsetdB(f) = \begin{cases} 1 + 0.4 \times \frac{f_{3dB} - f}{f_{3dB}}, & f < f_{3dB} \\ 1, & f \ge f_{3dB} \end{cases}$$

The inband PSD for $0 < f < 1.5$ MHz shall be measured with a 10 kHz resolution bandwidth.

f_{int} is the frequency where the two functions governing $PSDMASK_{SHDSL}(f)$ intersect in the frequency range from 0 to f_x. PBO is the power backoff value in dB. K_{SHDSL}, *Order*, f_x, $f_{3\,dB}$ and P_{SHDSL} are defined in Table B-13. P_{SHDSL} is the range of power in the transmit PSD with 0 dB power backoff. *R* is the payload data rate.

TABLE B-13

Asymmetric PSD parameters

Payload Date Rate (kbit/s)	Transmitter	K_{SHDSL}	*Order*	f_x (Hz)	$f_{3\,dB}$ (Hz)	P_{SHDSL} (dBm)
2 048	STU-C	16.86	7	1370667	548267	16.25
2 048	STU-R	15.66	7	685333	342667	16.50
2 304	STU-C	12.48	7	1541333	578000	14.75
2 304	STU-R	11.74	7	770667	385333	15.25

For 0 dB power backoff, the measured transmit power into 135 Ω shall fall within the range $P_{SHDSL} \pm 0.5$ dB. For power backoff values other than 0 dB, the measured transmit power into 135 Ω shall fall within the range $P_{SHDSL} \pm 0.5$ dB minus the power backoff value in dB. The measured transmit PSD into 135 Ω shall remain below $PSDMASK_{SHDSL}(f)$.

Figure B-9 shows the PSD masks with 0 dB power backoff for payload data rates of 2 048 and 2 304 kbit/s.

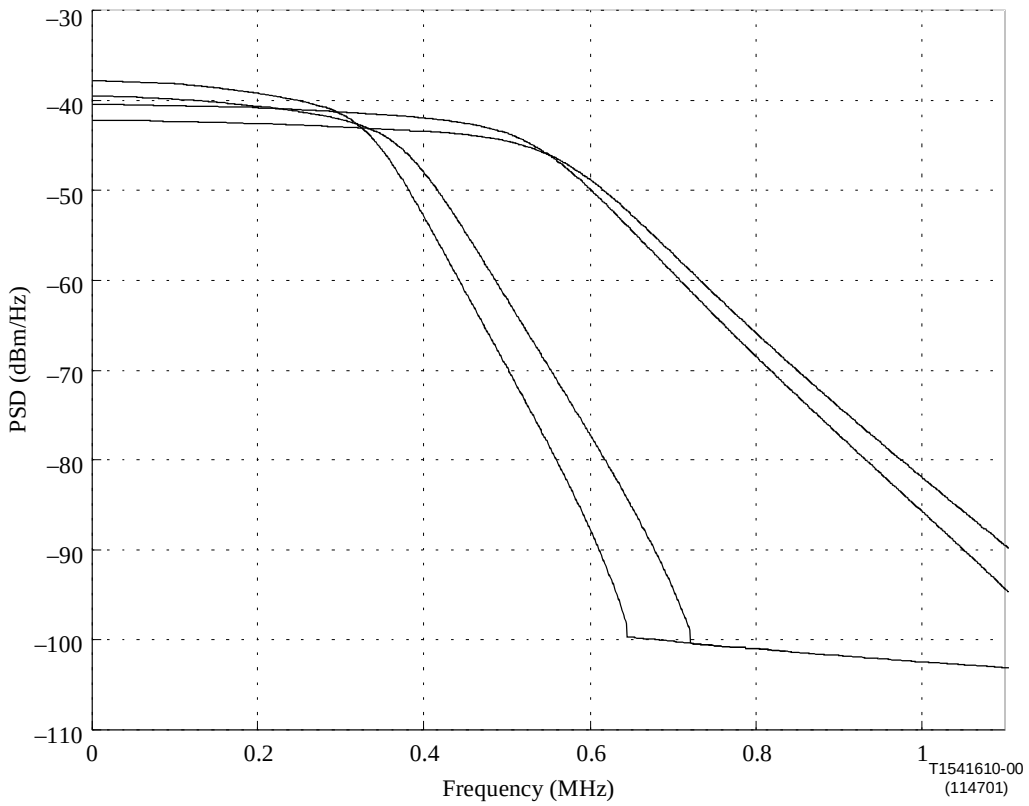


FIGURE B-9

PSD Masks for 0 dB Power Backoff

The equation for the nominal PSD measured at the terminals is:

$$NominalPSD(f) = \begin{cases} 10^{\frac{-PBO}{10}} \times \frac{K_{SHDSL}}{135} \times \frac{1}{f_x} \times \frac{\left[\sin\left(\frac{\pi f}{f_x}\right)\right]^2}{\left(\frac{\pi f}{f_x}\right)^2} \times \frac{1}{1+\left(\frac{f}{f_{3dB}}\right)^{2\times Order}} \times \frac{f^2}{f^2+f_c^2}, & f < f_{\text{int}} \\ 0.5683\times 10^{-4} \times f^{-1.5}, & f_{\text{int}} \le f \le 1.5\text{MHz} \\ -90\,\text{dBm/Hz peak with maximum power in a } [f,\ f+1\text{MHz}] \text{ window of -50 dBm}, & 1.5\text{MHz} < f \le 11.04\text{MHz} \end{cases}$$

where f_c is the transformer cutoff frequency, assumed to be 5 kHz. Figure B-10 shows the nominal transmit PSDs with 0 dB power backoff for payload data rates of 2 048 and 2 304 kbit/s.
NOTE - The nominal PSD is given for information only.

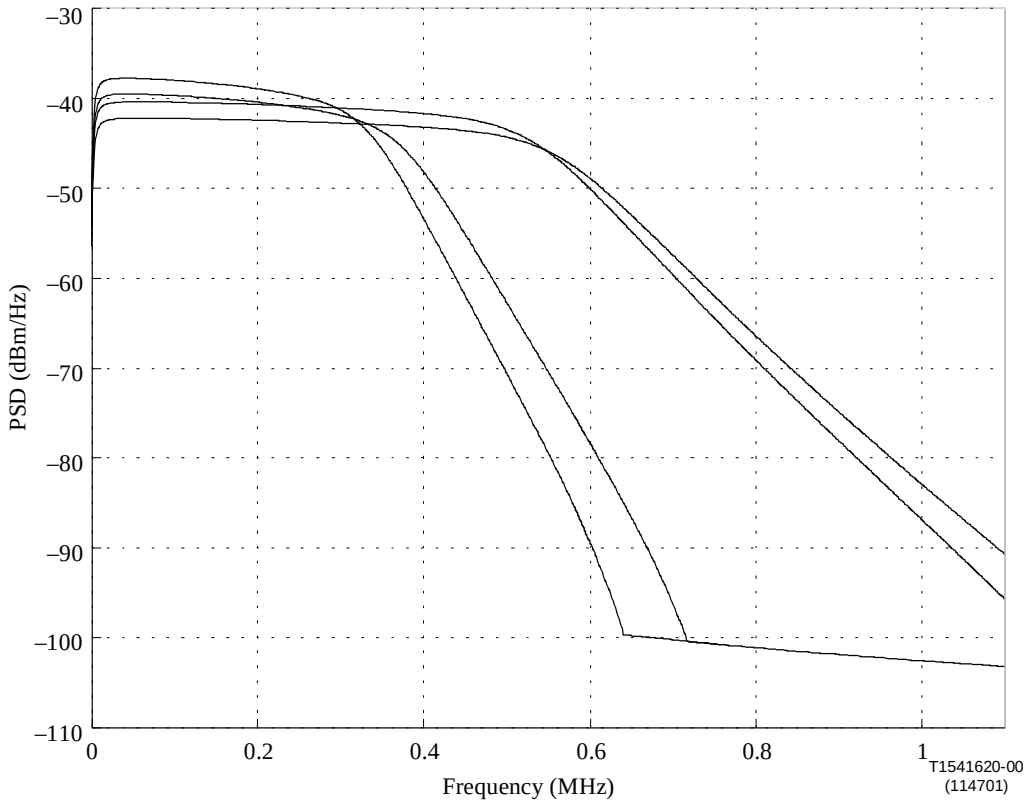


FIGURE B-10

Nominal Asymmetric PSDs for 0 dB Power Backoff

NOTE: In this section, *PSDMASK(f)* and *NominalPSD(f)* are in units of W/Hz unless otherwise specified, and *f* is in units of Hz.

B.5 Region-Specific Functional Characteristics

B.5.1 Data Rate

For devices supporting Annex B functionality, no additional limitation on data rates shall be placed beyond the limitations stated in § 5 and reiterated in § 7.1.1, § 8.1, and § 8.2. For details of the supported symbol rates and their association with PSDs, see § B.4.

B.5.2 Return Loss

For devices supporting Annex B functionality, return loss shall be specified based on the methodology of § 11.3 and the limitations of Figure 11-6. The following definitions shall be applied to the quantities shown in Figure 11-6:

$$RL_{MIN} = 14 \text{ dB}$$

$$f_0 = 3.99 \text{ kHz}$$

$$f_1 = 20 \text{ kHz}$$

$$f_2 = f_{sym}/2$$

$$f_3 = 2.51 f_{sym}$$

where f_{sym} is the symbol rate.

B.5.3 Span Powering

B.5.3.1 General

This section deals with power feeding of the STU-R, regenerators (if required) and the provision of power to the application interface for narrow-band services under restricted conditions (life line circuit). The requirements given in this clause imply compliance to IEC 60 950 [7].

B.5.3.2 Power Feeding of the STU-R

The STU-R shall be able to consume power from the remote power feeding circuit when the local power supply fails.

NOTE - The remote feeding strategy may not be applicable for extremely long lines or lines including regenerators. In those cases specific feeding methods may be applied, which are for further study.

The STU-R shall draw between 200 µA and up to a maximum of 3 mA as wetting current from the remote feeding circuit when the STU-R is being powered locally. When the local power fails the maximum current drawn by the STU-R from the remote feeding circuit shall be limited to the value specified in IEC 60 950 [7].

B.5.3.3 Power Feeding of the Interface for Narrow-band Services

When simultaneous telephone service is provided by the STU-R, feeding of restricted mode power for life line service has to be provided for at least one telephone set in case of local power failure.

NOTE - The remote feeding strategy may not be applicable for extremely long lines or lines including regenerators. In those cases specific feeding methods may be applied which are for further study.

B.5.3.4 Feeding Power from the STU-C

The feeding power shall be limited to the values specified by the TNV requirements in IEC 60 950 [7].

NOTE - This means that the sum of the DC- and AC-voltage at the STU-R may not exceed 120 V. The safety standards may for extraordinary cases with long lines or regenerators allow higher power to be supplied from the STU-C. This is left for further study. It is likely that supporting long lines and/or regenerators may imply floating (not connected to ground) power feeding circuits.

B.5.3.5 Power Available at the STU-R

The STU-R shall be able to deal with any polarity. With a minimum voltage of 45 V (see NOTE) at the input of the STU-R, it shall enter a full operational state.

NOTE - This value depends on the supply voltage and is for further study.

When remote power feeding is provided by the network, the STU-R and the side of the SRU directed towards the STU-C shall enter a high impedance state within 2 s after interruption of the remote current fed towards the STU-R or the SRU respectively. This state shall be maintained as long as the voltage on the line stays below 18 V (DC + AC peak). In this state the leakage current shall be less than 10 µA and the capacitance shall be greater than 2 µF. A guard time of at least 2 s between removing the remote power and applying a test voltage is necessary.

B.5.4 Longitudinal Balance

For devices supporting Annex B functionality, longitudinal balance shall be specified based on the methodology of § 11.1 and the limitations of Figure 11-2. The following definitions shall be applied to the quantities in Figure 11-2.

$$LB_{MIN} = 40dB$$

$$f_1 = 5kHz$$

$$f_2 = f_{sym}/2$$

where f_{sym} is the symbol rate.

B.5.5 Longitudinal Output Voltage

For devices supporting Annex B functionality, longitudinal output voltage shall be specified based on the methodology of § 11.2. The measurement frequency range shall be between 100 Hz and 400 kHz.

B.5.6 PMMS Target Margin

If the optional line probe is selected during the G.994.1 session, the receiver shall use the negotiated target margin. If worst-case PMMS target margin is selected, then the receiver shall assume the disturbers of Table B-14 to determine if a particular rate can be supported. Reference crosstalk shall be computed using the cable crosstalk models of § B.3.5.2, assuming infinite loop length so that FEXT components are ignored and NEXT is independent of loop length. The reference crosstalk specified in this section may not be representative of worst-case conditions in all networks. Differences between crosstalk environments may be compensated by adjusting the target margin.

TABLE B-14

Reference Disturbers Used During PMMS for Worst-Case Target Margin

Rate (kbit/s)	PSD (direction)	Reference disturber
all	symmetric (US/DS)	49 SHDSL
2 048	asymmetric (US)	49 SHDSL-SYM with f_{sym}=685 333 Hz
2 048	asymmetric (DS)	49 SHDSL-SYM with f_{sym}=685 333 Hz
2 304	asymmetric (US)	49 SHDSL-SYM with f_{sym}=770 667 Hz
2 304	asymmetric (DS)	49 SHDSL-SYM with f_{sym}=770 667 Hz

ANNEX C

Regional Requirements - Region 3

See G.992.1, Annex H [1] for specifications of transceivers for use in networks with existing TCM-ISDN service (as specified in G.961, Appendix III [B1]).

ANNEX D

Signal Regenerator Operation

In order to achieve data transmission over greater distances than are achievable over a single SHDSL segment, one or more signal regenerators (SRUs) may be employed. In the optional two-pair mode, two-pair regenerators may be used when this reach extension is required. This Annex specifies operational characteristics of signal regenerators and the start-up sequence for SHDSL spans containing signal regenerators. Additional explanatory text is included in Appendix III.

D.1 Reference Diagram

Figure D-1 is a reference diagram of a SHDSL span containing two regenerators. Up to eight (8) regenerators per span are supported within the EOC addressing scheme (§ 9.5.5.5), and no further limitation is intended herein. Each SRU shall consist of two parts: an SRU-R for interfacing with the STU-C (or a separate SRU-C), and an SRU-C for interfacing with the STU-R (or a separate SRU-R). An internal connection between the SRU-R and SRU-C shall provide the communication between the two parts during start-up and normal operation. An SHDSL span containing X regenerators shall contain $X + 1$ separated SHDSL segments, designated TR1 (STU-C to SRU_1), TR2 (SRU_X-C to STU-R), and RRn (SRU_n-C to SRU_{n+1} – R, where $1 \leq n \leq X$-1). Each segment shall follow the general principles described in § 6.2, § 6.3 and § 7.2 for the preactivation and activation procedures. Additional requirements specific to spans containing regenerators are described in this Annex.

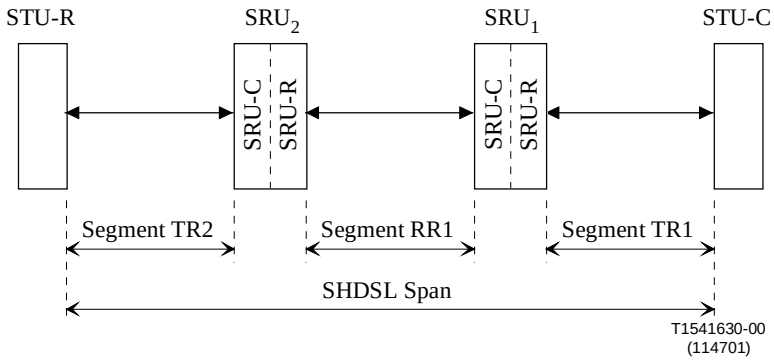


FIGURE D-1

Block Diagram of a SHDSL Span with Two Signal Regenerators

D.2 Startup Procedures

D.2.1 SRU-C

Figure D-2 shows the State Transition Diagram for SRU-C start-up and operation. The SRU-C begins in the "Idle" state and, in the case of an STU-R initiated start-up, transitions first to the "Wait for STU-C" state. For an STU-C initiated start-up, the SRU-C moves from "Idle" to the "G.994.1

Session 1" state. An SRU initiated start-up shall function identically to an STU-C initiated start-up from the perspective of the SRU-C.

The SRU-C shall communicate "Capabilities Available" status and transfer a list of its capabilities to the SRU-R across the regenerator's internal interface upon entering the "Wait for STU-C" state. The SRU-C's capabilities list, as transferred to the SRU-R, shall be the intersection of its own capabilities, the capabilities list it received from the STU-R (or SRU-R) in its G.994.1 session, and the segment capabilities determined by the line probe, if used.

The SRU-C shall receive mode selection information from the SRU-R in association with the "SRU-R Active" indication. In the subsequent G.994.1 session, the SRU-C shall select the same mode and parameter settings for the SHDSL session.

The timer T_{SRUC} shall be set to 4 minutes. If T_{SRUC} expires before the SRU-C reaches the "Active" state, the SRU-C shall return to the "Idle" state and shall indicate link failure to the SRU-R across the internal interface. The SRU-C shall also indicate failure and return to the "Idle" state if a G.994.1 initiation is unsuccessful after 30 s.

The "Diagnostic Mode" bit, if set in the G.994.1 Capabilities Exchange, shall cause an SRU-C to function as an STU-C if the subsequent segment fails. This implies that an internal failure indication received while in the "Wait for STU-C" state shall cause the SRU-C to select an operational mode, initiate a G.994.1 session, and transition to state "G.994.1 Session 2".

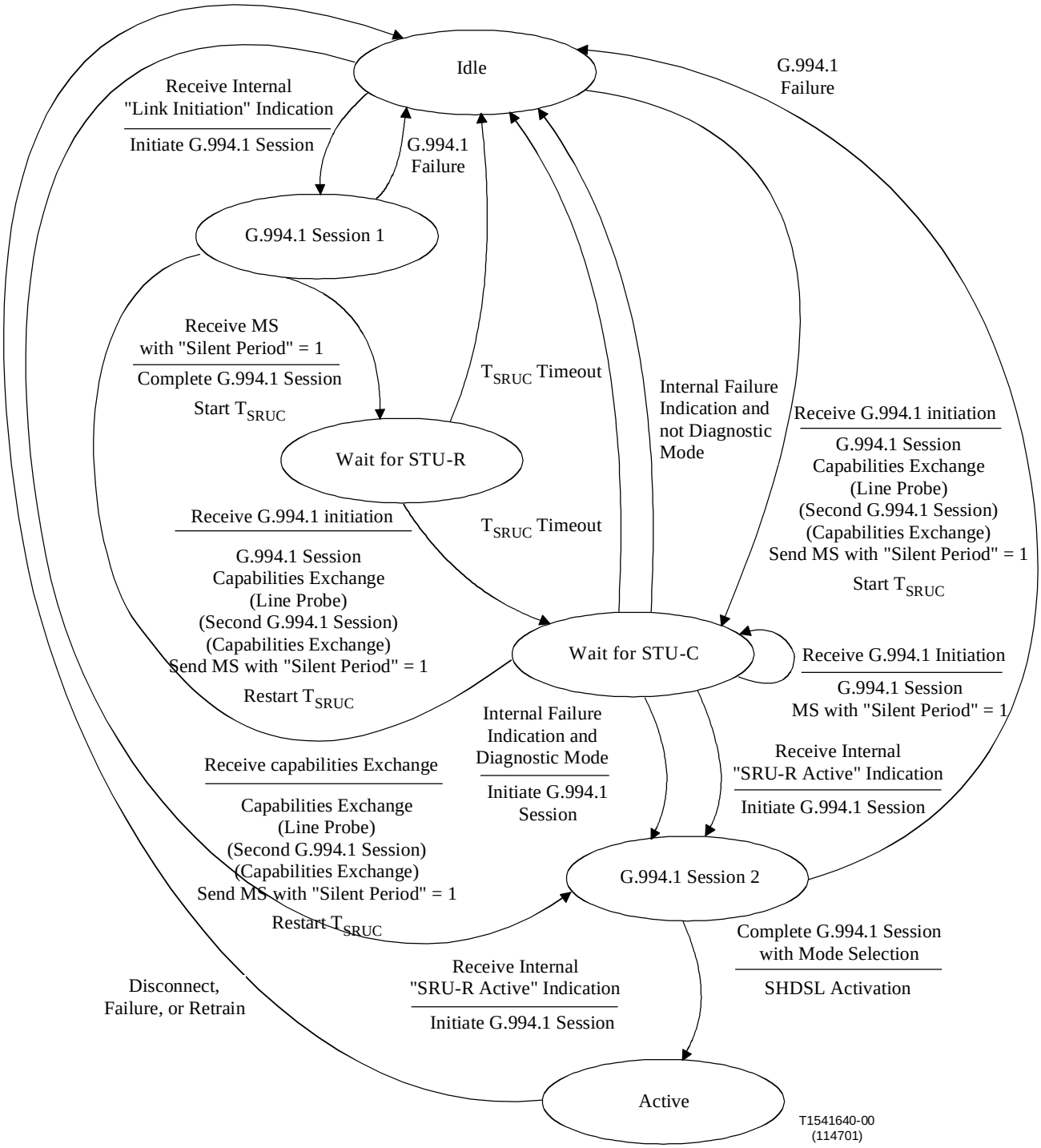


FIGURE D-2

SRU-C State Transition Diagram

D.2.2 SRU-R

Figure D-3 shows the State Transition Diagram for SRU-R start-up and operation. The SRU-R begins in the "Idle" state and, in the case of an STU-R initiated train, transitions first to the "G.994.1

Session 1" state. For an STU-C initiated train, the SRU-C moves from "Idle" to the "G.994.1 Session 2" state.

The SRU-R shall communicate "Link Initiation" status to the SRU-C across the regenerator's internal interface upon entering the "Wait for STU-R" state. Upon entering the "Active" state, it shall communicate "SRU-R Active" status to the SRU-C. If plesiochronous operation (Clock Mode 1; see § 10) is selected, the SRU-R may optionally indicate its entry into the "Active" state to the SRU-C prior to the completion of the SHDSL activation sequence. If synchronous or network referenced plesiochronous clocking is selected (Clock Modes 2, 3a or 3b; see § 10), the SRU-R shall not indicate entry into the "Active" state until the SHDSL activation sequence has been completed.

The SRU-R shall receive a list of capabilities from the SRU-C across the regenerator's internal interface in association with the "Capabilities Available" indication. The SRU-R's capabilities list, as indicated in the subsequent G.994.1 session, shall be the intersection of its own capabilities with the capabilities list it received from the SRU-C.

The SRU-R shall provide mode selection information to the SRU-C in association with the "SRU-R Active" indication, based on the selections it has received in the G.994.1 session.

The timer T_{SRUR} shall be set to 4 minutes. If T_{SRUR} expires before the SRU-R reaches the "Active" state, the SRU-R shall return to the "Idle" state and shall indicate link failure to the SRU-C across the internal interface. The SRU-R shall also indicate failure and return to the "Idle" state if a G.994.1 initiation is unsuccessful after 30 s.

The "Diagnostic Mode" bit, if set in the G.994.1 Capabilities Exchange, shall cause an SRU-R to function as an STU-R if the subsequent segment fails. This implies that an internal failure indication received while in the "Wait for STU-R" state shall cause the SRU-R to initiate a G.994.1 session and transition to state "G.994.1 Session 2".

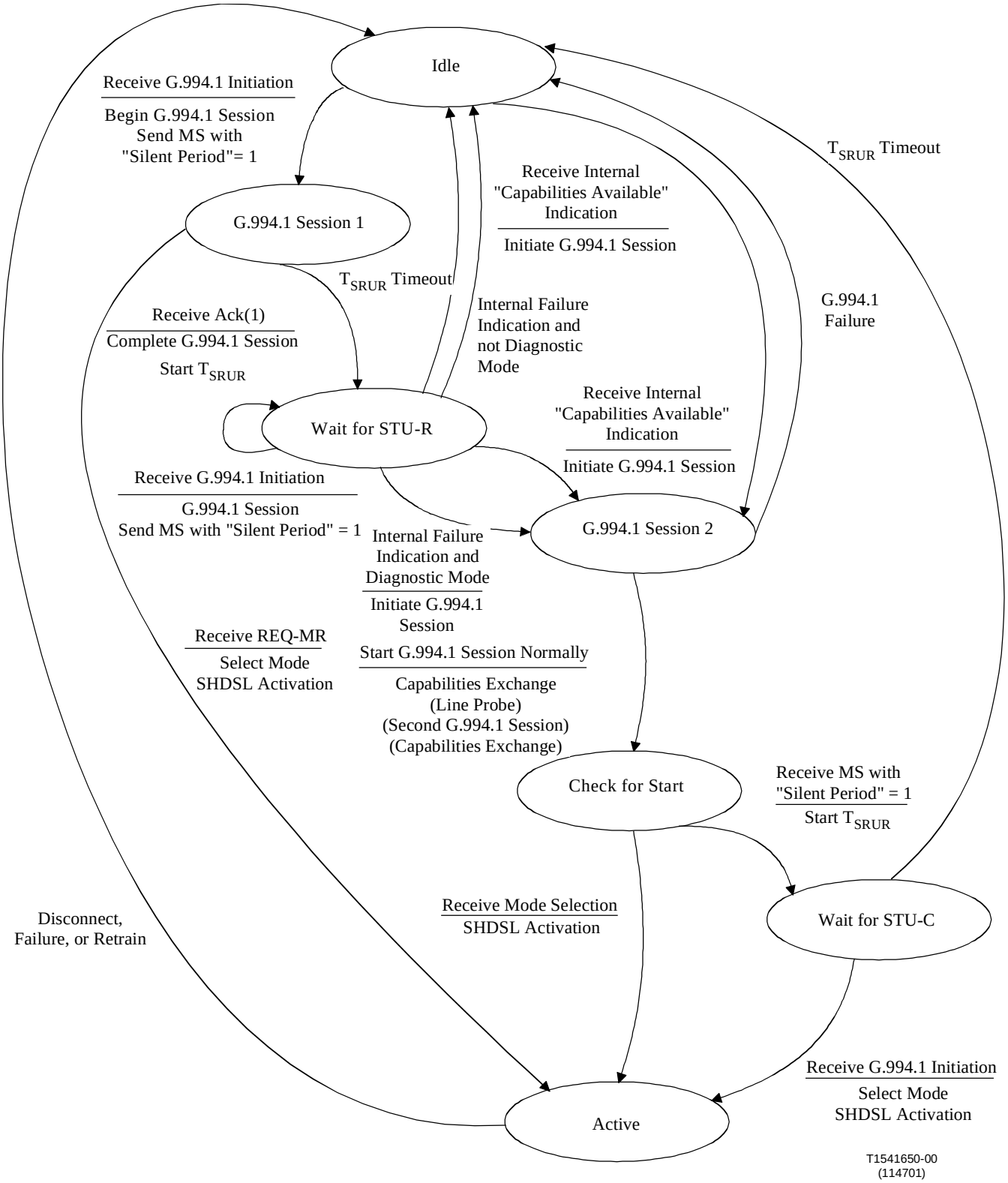


FIGURE D-3

SRU-R State Transition Diagram

D.2.3 STU-C

In order to support operation with regenerators, each STU-C shall support the Regenerator Silent Period (RSP) bit, as specified in G.994.1. Second, the STU-C shall not indicate a training failure or error until it has been forced into "silent" mode for at least 5 consecutive minutes.

D.2.4 STU-R

In order to support operation with regenerators, each STU-R shall support the Regenerator Silent Period (RSP) bit, as specified in G.994.1. The STU-R shall not indicate a training failure or error until it has been forced into "silent" mode for at least 5 consecutive minutes.

D.2.5 Segment Failures and Retrains

In the case of a segment failure or a retrain, each segment of the span shall be deactivated, with each SRU-C and each SRU-R returning to its "Idle" state. The restart may then be initiated by the SRU, the STU-R, or the STU-C.

D.3 Symbol Rates

For Annex A operational modes, signal regenerators may transmit at symbol rates up to and including 280 ksymbol/s in either two-wire or the optional four-wire mode. This corresponds, for 16-TCPAM, to maximum user data rates (not including framing overhead) of 832 kbit/s and 1 664 kbit/s for two-wire and four-wire operation, respectively. Operation at higher symbol rates is for further study.

For Annex B operational modes, signal regenerators may transmit at symbol rates up to and including 685.33 ksymbol/s in either two-wire or the optional four-wire mode. This corresponds, for 16-TCPAM, to maximum user data rates (not including framing overhead) of 2.048 Mbit/s and 4.096 Mbit/s for two-wire and four-wire operation, respectively. Operation at higher symbol rates is for further study.

In either case, each STU and SRU on a span shall select the same operational data rate.

D.4 PSD Masks

Any of the PSDs from Annex A or Annex B may be used for the TR1 segment (STU-C to SRU_1-R), as appropriate to the given region. All other segments shall employ one of the appropriate symmetric PSDs, as described in either § A.4.1 or § B.4.1. The selection of PSD shall be limited by the symbol rate considerations of § D.3.

ANNEX E

Application-specific TPS-TC Framing

This Annex provides implementation details for the various types of TPS-TC framing that may be supported by SHDSL transceivers. The TPS-TC framing mode is selected during preactivation, but the criteria for selecting a particular TPS-TC mode are application specific and are beyond the scope of this Recommendation.

E.1 TPS-TC for Clear Channel Data

In Clear Channel mode, there shall be no specified relationship between the structure of the user data and its positioning within the Payload Sub-Blocks. k_s bits of contiguous user data shall be contained within each Sub-Block, as specified in § 8.1. The temporal relationship between the user data stream and the data within the Sub-Blocks shall be maintained such that the order of bits in time from the user data stream shall match the order of transmission within the SHDSL Payload Sub-Blocks. Any additional structure within the user data shall be maintained by an unspecified higher layer protocol and is outside the scope of this Recommendation.

In the optional four-wire mode, clear channel data will be carried over both pairs using interleaving, as described in § 8.2. k_s bits of contiguous user data shall be contained within a Sub-Block on Pair 1, and the following k_s bits of contiguous user data shall be contained within the corresponding Sub-Block on Pair 2. As noted above, any additional structure within the user data shall be maintained by an unspecified higher layer protocol and is outside the scope of this Recommendation.

E.2 TPS-TC for Clear Channel Byte-Oriented Data

In the byte-oriented clear channel mode, the input byte stream shall be aligned within the SHDSL Payload Sub-Block such that the byte boundaries are preserved. Each Payload Sub-Block is treated as containing n 8-bit time slots. Each byte from the input data stream is mapped LSB-first into the next available time slot. The first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, …, time slot n. k_s bits (or n bytes) of contiguous data shall be contained within each Sub-Block, as specified in §8.1. $k_s = i + n \times 8$, and, in this mode, $i = 0$ and $3 \leq n < 36$. See Figure E-1 for additional details.

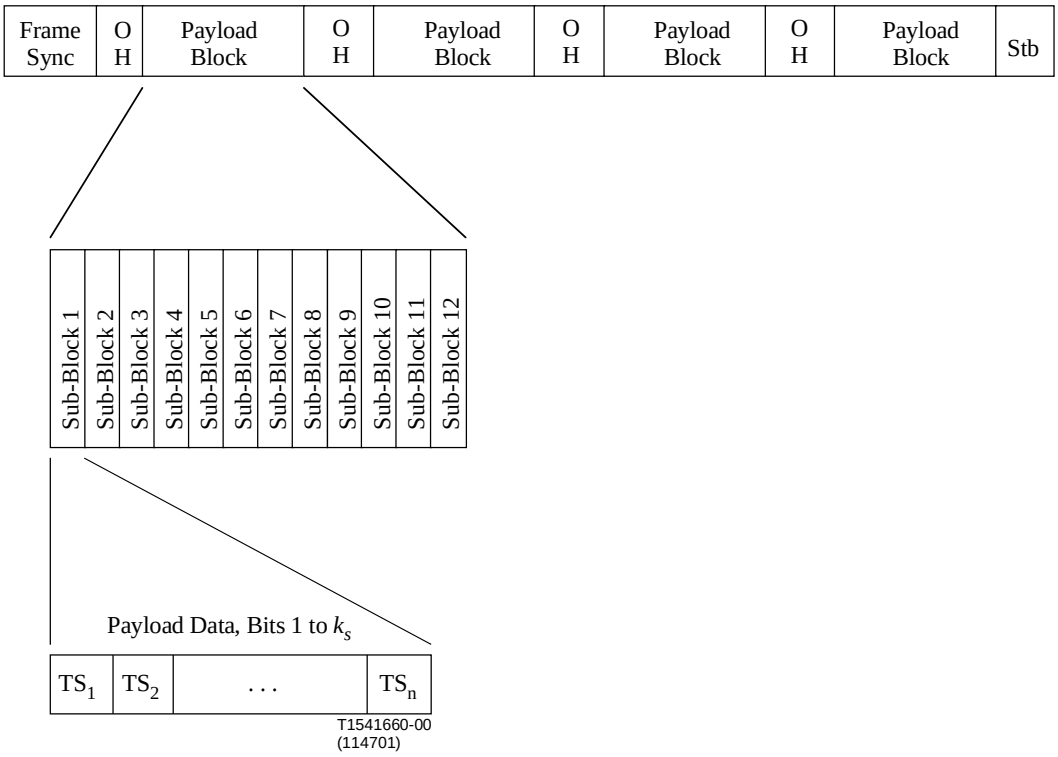


FIGURE E-1

Clear Channel Byte-Oriented Framing

In the optional four-wire mode, byte-oriented data is carried over both pairs using interleaving, as described in § 8.2. A total of $2k_s$ bits ($2n$ bytes) of byte-oriented data shall be transported per SHDSL Payload Sub-Block. $k_s = i + n\times8$, and, in this mode, $i = 0$ and $3 \le n \le 36$. Only even numbers of time slots may be supported in four-wire mode. The input byte stream shall be aligned within the SHDSL Payload Sub-Block such that the byte boundaries are preserved. Each Payload Sub-Block is treated as containing $2n$ 8-bit time slots. Each byte from the input data stream is mapped LSB-first into the next available time slot. The first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, …, time slot n. $2k_s$ bits (or $2n$ bytes) of contiguous data shall be contained within each Sub-Block, as specified in §8.1. $k_s = i + n\times8$, and, in this mode, $i = 0$ and $3 \le n < 36$. The bytes from the input data stream shall be interleaved between Pair 1 and Pair 2, such that the odd numbered bytes are carried on Pair 1 and the even numbered bytes are carried on Pair 2. See Figure E-2 for additional details.

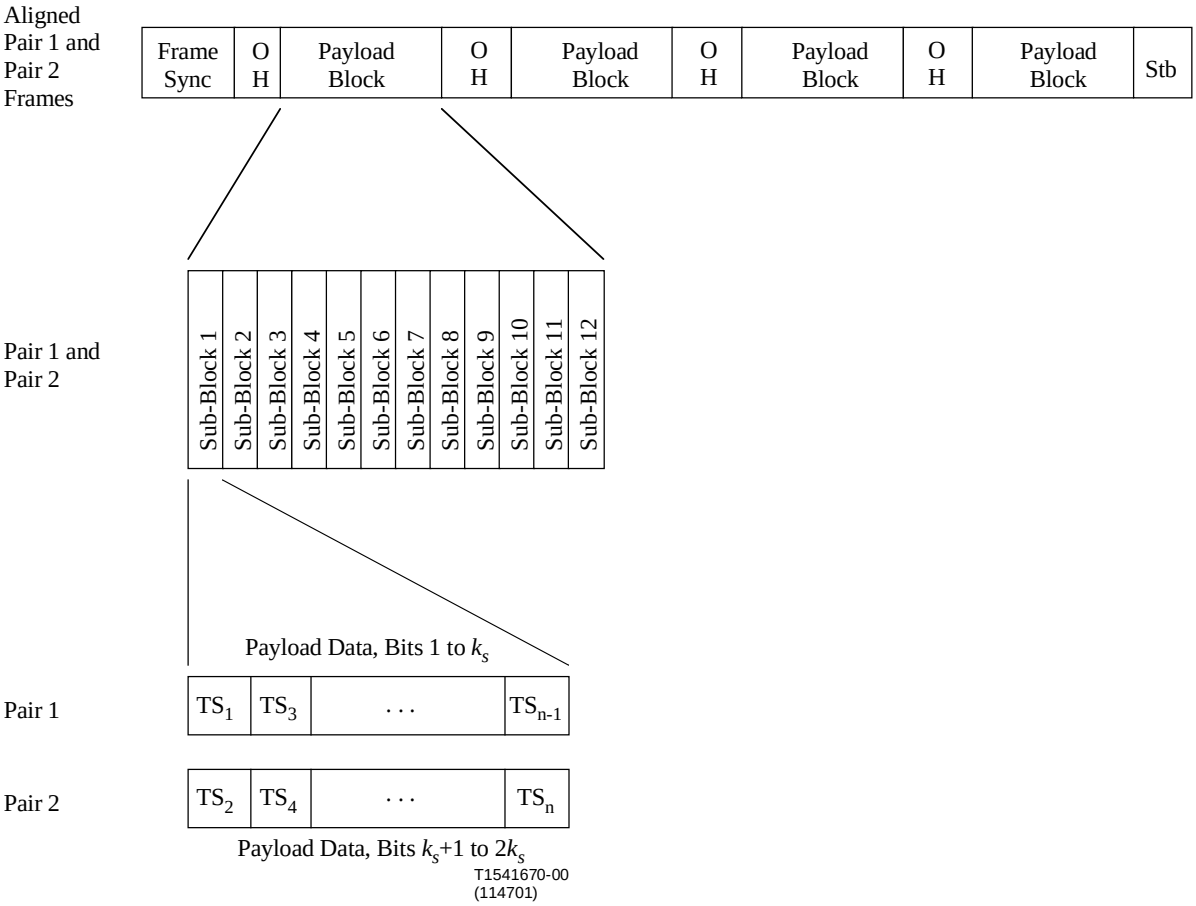


FIGURE E-2

Four-wire Framing for Byte-Oriented Clear Channel

E.3 TPS-TC for Unaligned DS1 Transport

Much of the data within the North American network is structured as "DS1" data streams, which, for purposes of this Recommendation, can be described as 1.544 Mbit/s data streams containing 8 kHz framing, with each frame containing 24 8-bit time slots and one framing bit. Details of DS1 framing and associated data structure can be found in G.704 § 2.1 [B6].

In Unaligned DS1 mode, there shall be no specified relationship between the DS1 frames and their positioning within the Payload Sub-Blocks. k_s bits of contiguous data shall be contained within each Sub-Block, as specified in § 8.1. $k_s = i + n \times 8$, and, in this mode, $n = 24$ and $i = 1$. The DS1 framing clocks shall be synchronized to the SHDSL clocks such that the DS1 frame always appears in the same position within each SHDSL Payload Sub-Block; however, no particular alignment is specified. The temporal relationship between the DS1 data stream and the data within the Sub-Blocks shall be maintained, such that that the order of bits in time from the DS1 data stream shall match the order of transmission within the SHDSL Payload Sub-Blocks. The optional four-wire mode will not support Unaligned DS1 transport.

E.4 TPS-TC for Aligned DS1/Fractional DS1 Transport

As noted in § E.3, "DS1" data streams consist of 1.544 Mbit/s data streams containing 8 kHz framing, with each frame containing 24 8-bit time slots and one framing bit. In some cases, "Fractional DS1" data streams are used, where DS1 frames contain less than the normal 24 8-bit time slots.

In Aligned DS1/Fractional DS1 mode, each DS1 frame shall be aligned within the SHDSL Payload Sub-Block such that the DS1 framing bit occupies the first bit position within the Payload Sub-Block, followed by time slot 1, time slot 2, …, time slot n. k_s bits of contiguous data shall be contained within each Sub-Block, as specified in § 8.1. $k_s = i + n \times 8$, and, in this mode, $i = 1$. In DS1 applications, $n = 24$, and, in Fractional DS1 applications, $3 \leq n < 24$. The DS1 framing clocks shall be synchronized to the SHDSL clocks such that the DS1 frame always appears in the defined position within each SHDSL Payload Sub-Block. See Figure E-3 for additional details.

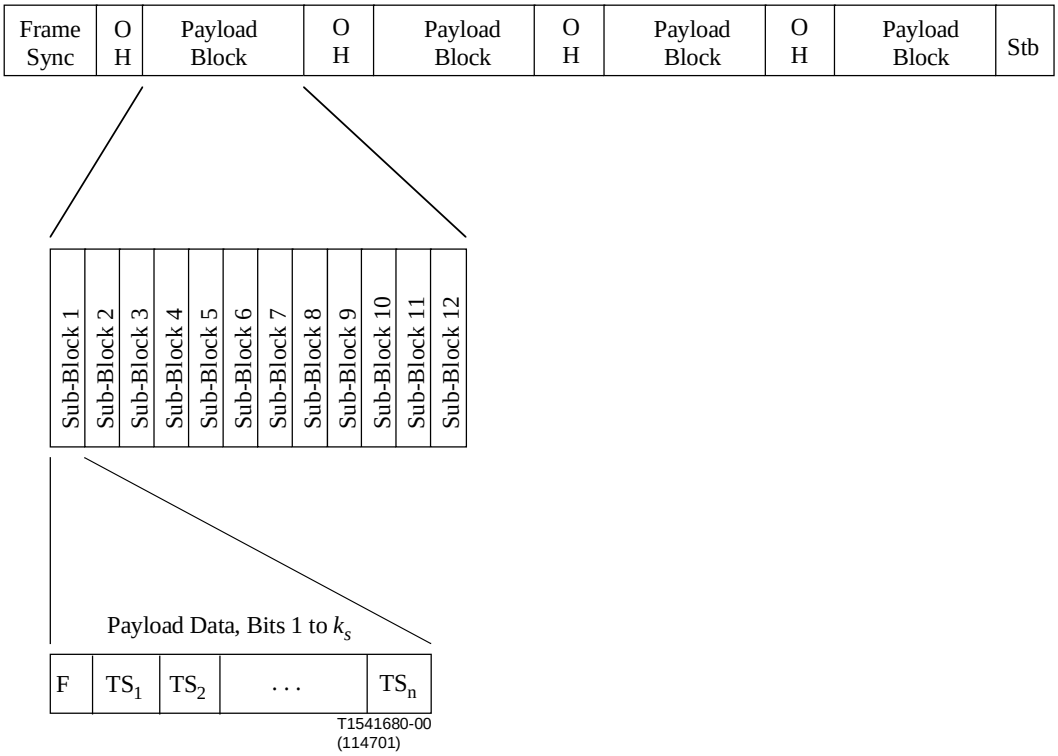


FIGURE E-3

Aligned DS1/Fractional DS1 Framing

In the optional four-wire mode, DS1 / Fractional DS1 data will be carried over both pairs using interleaving, as described in § 8.2. A total of $2k_s$-1 bits of DS1 / Fractional DS1 data shall be transported per SHDSL Payload Sub-Block. $k_s = i + n \times 8$, and, in this mode, $i = 1$. In DS1 applications, $n = 12$, and in Fractional DS1 applications, $3 \leq n < 12$. Only even numbers of DS1 time slots may be supported in four-wire mode. Each DS1 frame shall be aligned within the SHDSL Payload Sub-Block such that the DS1 framing bit occupies the first bit position within the Payload Sub-Block on both Pair 1 and Pair 2. The time slots of the DS1 frame shall be interleaved between Pair 1 and Pair 2, such that the odd numbered time slots are carried on Pair 1 and the even numbered time slots are carried on Pair 2. See Figure E-4 for additional details.

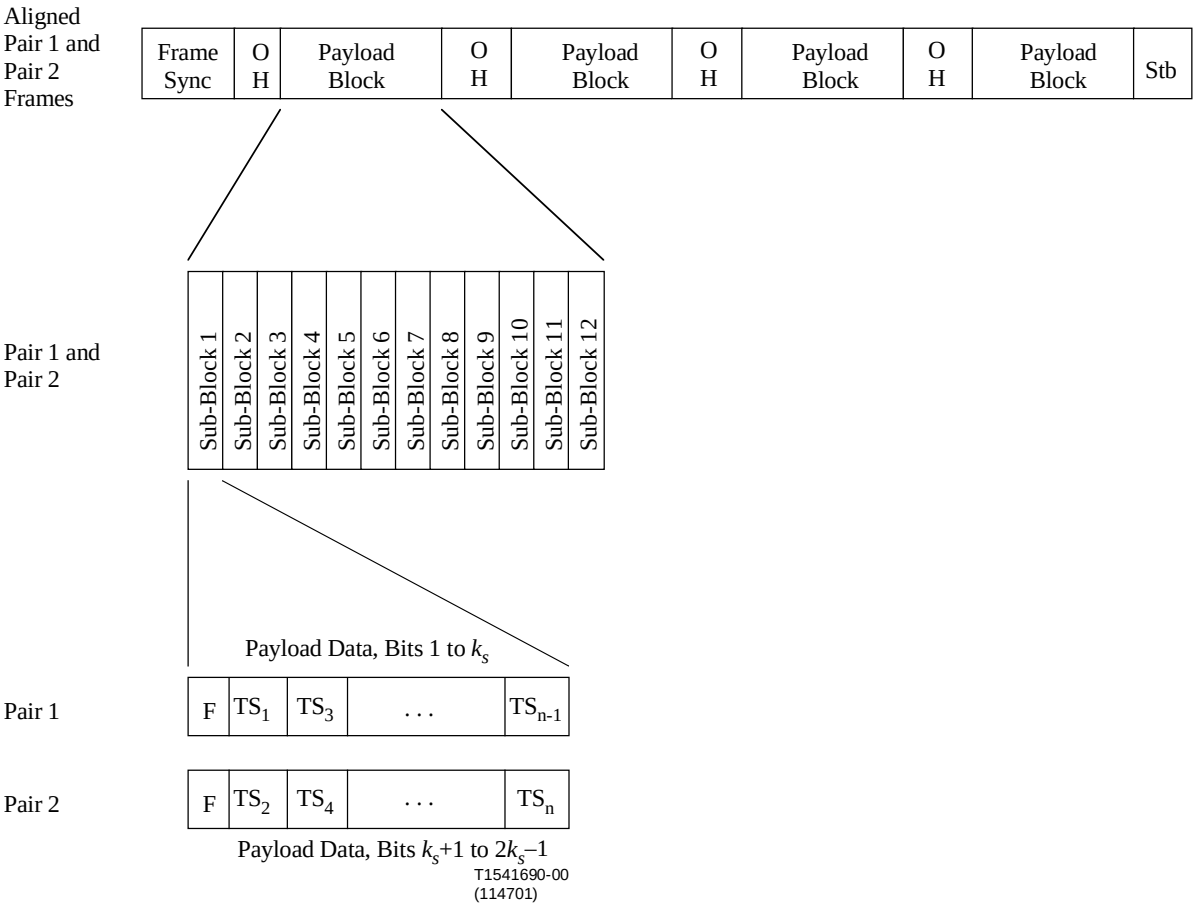


FIGURE E-4

Four-wire Framing for DS1/Fractional DS1

E.5 TPS-TC for European 2 048 kbit/s Digital Unstructured Leased Line (D2048U)

D2048U data streams contain unstructured 2.048 Mbit/s data with no specified framing. These data streams shall be carried using the Clear Channel TPS-TC described in § E.1.

E.6 TPS-TC for Unaligned European 2 048 kbit/s Digital Structured Leased Line (D2048S)

Much of the data within the European network is structured as D2048S data streams, which, for purposes of this Recommendation, can be described as 2.048 Mbit/s data streams containing 8 kHz framing, with each frame containing 32 8-bit time slots. Details of D2048S framing and associated data structure can be found in G.704 § 2.3 [B6].

In Unaligned D2048S mode, there shall be no specified relationship between the D2048S frames and their positioning within the Payload Sub-Blocks. k_s bits of contiguous data shall be contained within each Sub-Block, as specified in § 8.1. $k_s = i + n \times 8$, and, in this mode, $n = 32$ and $i = 0$. The D2048S framing clocks shall be synchronized to the SHDSL clocks such that the D2048S frame always appears in the same position within each SHDSL Payload Sub-Block; however, no particular alignment is specified. The temporal relationship between the D2048S data stream and

the data within the Sub-Blocks shall be maintained, such that that the order of bits in time from the D2048S data stream shall match the order of transmission within the SHDSL Payload Sub-Blocks. The optional four-wire mode will not support Unaligned D2048S transport.

E.7 TPS-TC for Aligned European 2 048 kbit/s Digital Structured Leased Line (D2048S) and Fractional

As noted in § E.6, D2048S data streams consist of 2 048 Mbit/s data streams containing 8 kHz framing, with each frame containing 32 8-bit time slots. In some cases, Fractional D2048S data streams are used, where frames contain less than the normal 32 8-bit time slots.

In the aligned D2048S mode, each D2048S frame shall be aligned within the SHDSL Payload Sub-Block such that the first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, …, time slot *n*. k_s bits of contiguous data shall be contained within each Sub-Block, as specified in § 8.1. $k_s = i + n \times 8$, and, in this mode, $i = 0$. In D2048S applications, $n = 32$, and, in Fractional D2048S applications, $3 \leq n < 32$. The D2048S framing clocks shall be synchronized to the SHDSL clocks such that the D2048S frame always appears in the defined position within each SHDSL Payload Sub-Block. See Figure E-5 for additional details.

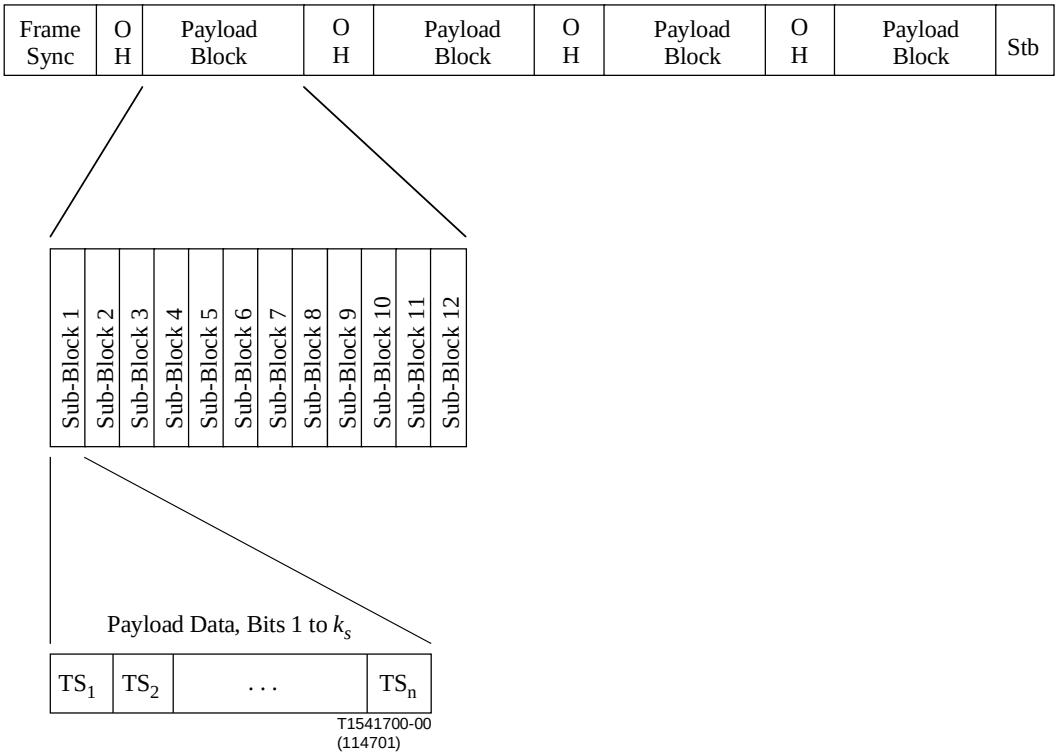


FIGURE E-5

Aligned D2048S/Fractional D2048S Framing

In the optional four-wire mode, D2048S/Fractional D2048S data will be carried over both pairs using interleaving, as described in § 8.2. A total of $2k_s$ bits of D2048S / Fractional D2048S data shall be transported per SHDSL Payload Sub-Block. $k_s = i + n \times 8$, and, in this mode, $i = 0$. In D2048S applications, $n = 16$, and in Fractional DS1 applications, $3 \leq n < 16$. Only even numbers of D2048S time slots may be supported in four-wire mode. The time slots of the D2048S frame shall

be interleaved between Pair 1 and Pair 2, such that the odd numbered time slots are carried on Pair 1 and the even numbered time slots are carried on Pair 2. See Figure E-6 for additional details.

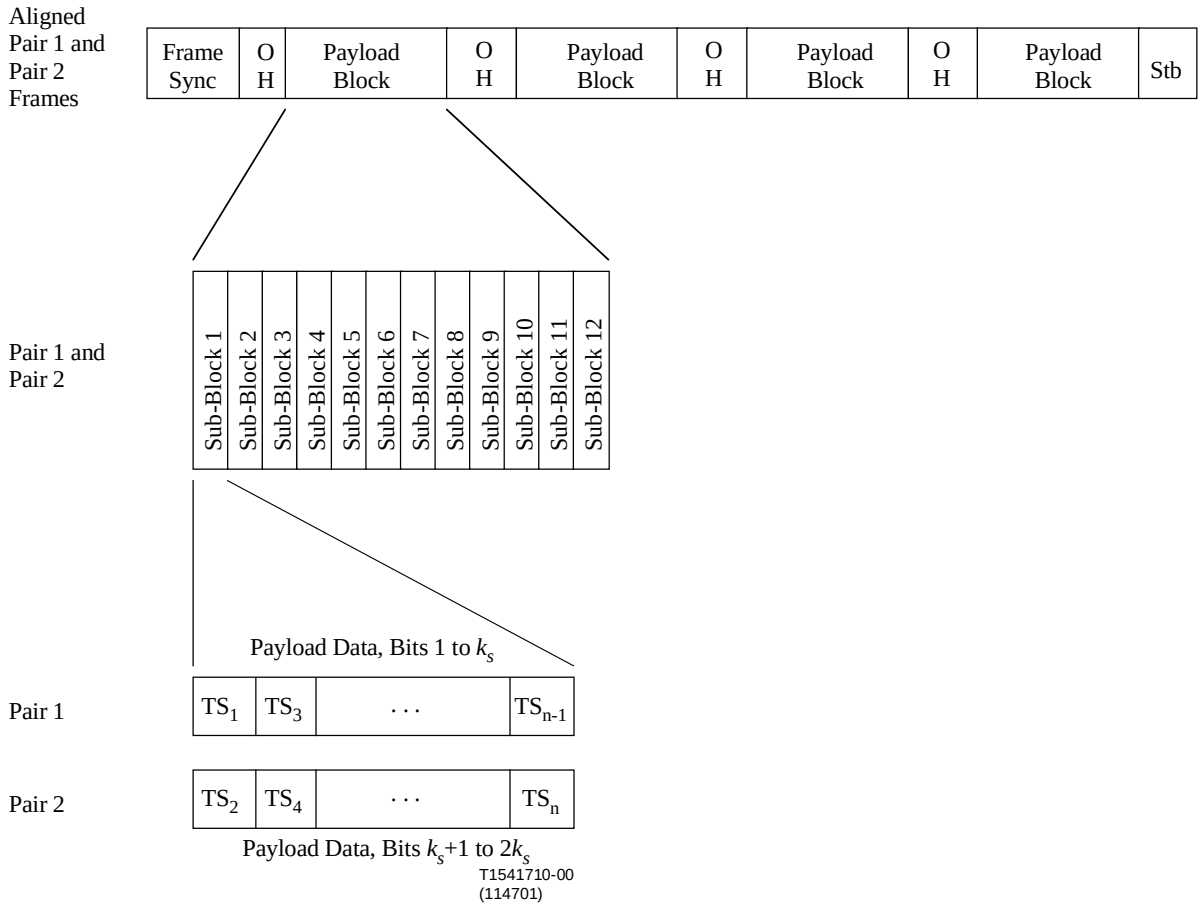


FIGURE E-6

Four-wire Framing for Aligned D2048S/Fractional D2048S

E.8 TPS-TC for Synchronous ISDN BRA

In this TPS-TC mode, the mapping of the ISDN customer data channels to SHDSL payload channels is specified for synchronous transport of multiple ISDN BRAs using clock mode 3a (see § 10.1).

The ISDN customer data channels are embedded into the payload data within the SHDSL frames. ISDN channels and SHDSL frames (and any other TPS-TC if Dual Bearer mode is utilized – see § E.10) are synchronized to the same clock domain.

E.8.1 ISDN BRA over SHDSL Frames

Figure E-7 illustrates typical transport of ISDN BRAs within the SHDSL frames. The basic characteristics of this transport are as follows:

- B channels and D channels are mapped on SHDSL payload channels.

- The ISDN BRA does not need a separate synchronization since the SHDSL frames are synchronized to the same clock domain. Therefore, the ISDN frame word (12 kbit/s) is not needed.
- The ISDN M-channel transports ISDN line status bits, transmission control information as well as signalling to control the ISDN connection. Only the ISDN M-channel functions which are needed to control the interface to the ISDN terminal equipment are transported over a messaging channel (SHDSL EOC or fast signalling channel).

E.8.2. Mapping of ISDN B- and D-Channels on SHDSL Payload Channels

The ISDN B- and D- channels are transported within the SHDSL payload sub-blocks. The SHDSL payload data is structured within the SHDSL frames as follows:

- Each payload sub-block contains $k_s = i + n \times 8$ bits (i = 0..7 and n = 3..36)
- Each sub-block is ordered in the following way: i 1-bit timeslots followed by n 8-bit timeslots
- 1-bit timeslots are referred to as Z-bits, and 8-bit timeslots are referred to as TS_1 ... TS_n.

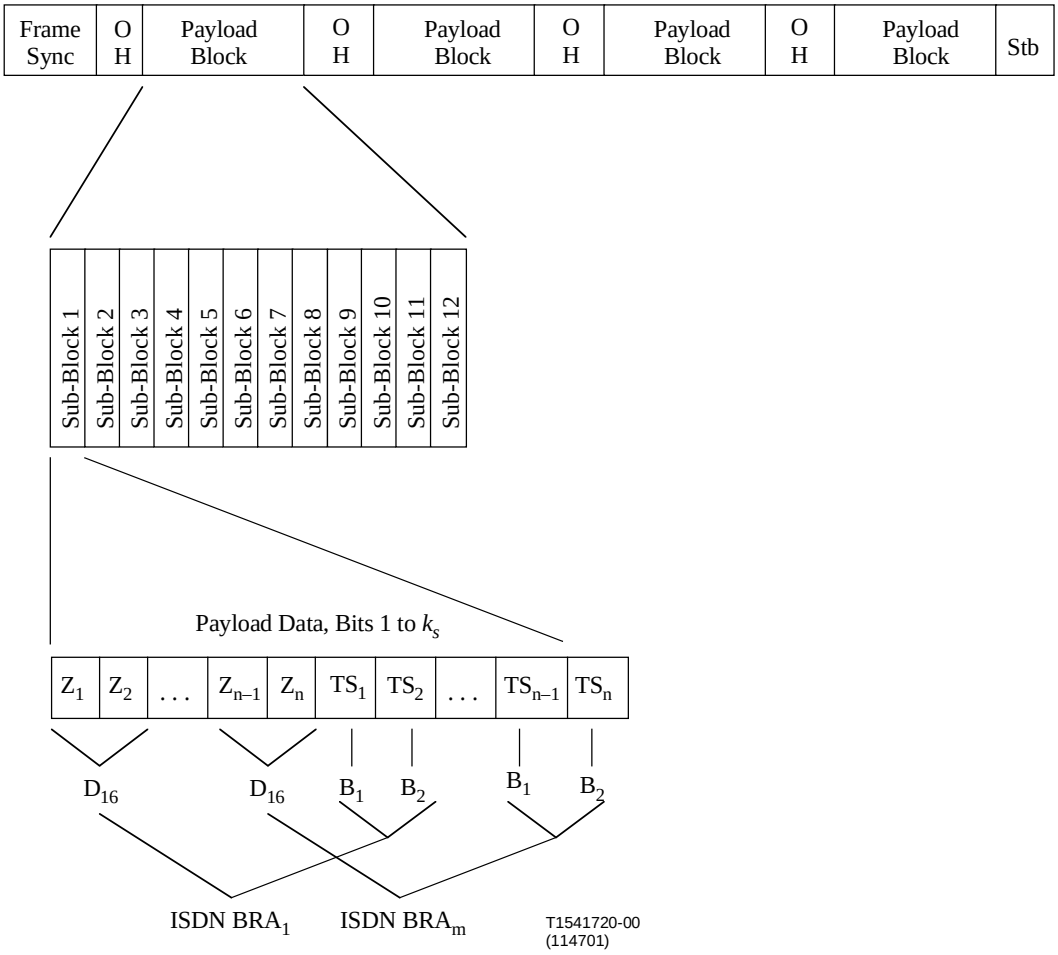


FIGURE E-7

Mapping of ISDN B- and D- Channels

The payload sub-blocks are composed of combinations of $n \times 8$bit TS timeslots and $i \times 1$bit Z-timeslots:

- *n* corresponds to the number of 64 kbit/s payload channels
- *i* corresponds to the number of 8 kbit/s channels

This payload structure allows efficient mapping of ISDN BRA channels on SHDSL frames.

- Data channels (64 kbit/s each, designated $B_1 – B_y$) are mapped onto 64 kbit/s TS-channels
- Signalling channels (16 kbit/s each, designated $D_1 – D_x$) are mapped onto two 8 kbit/s Z-channels each.[6]

A general example of this mapping technique is shown in Figure E-7.

E.8.3 Multi-ISDN BRAs

The transport of up to 6 ISDN BRAs is described in detail in the next paragraphs. Figure E-8 shows a mapping example for two ISDN BRAs.

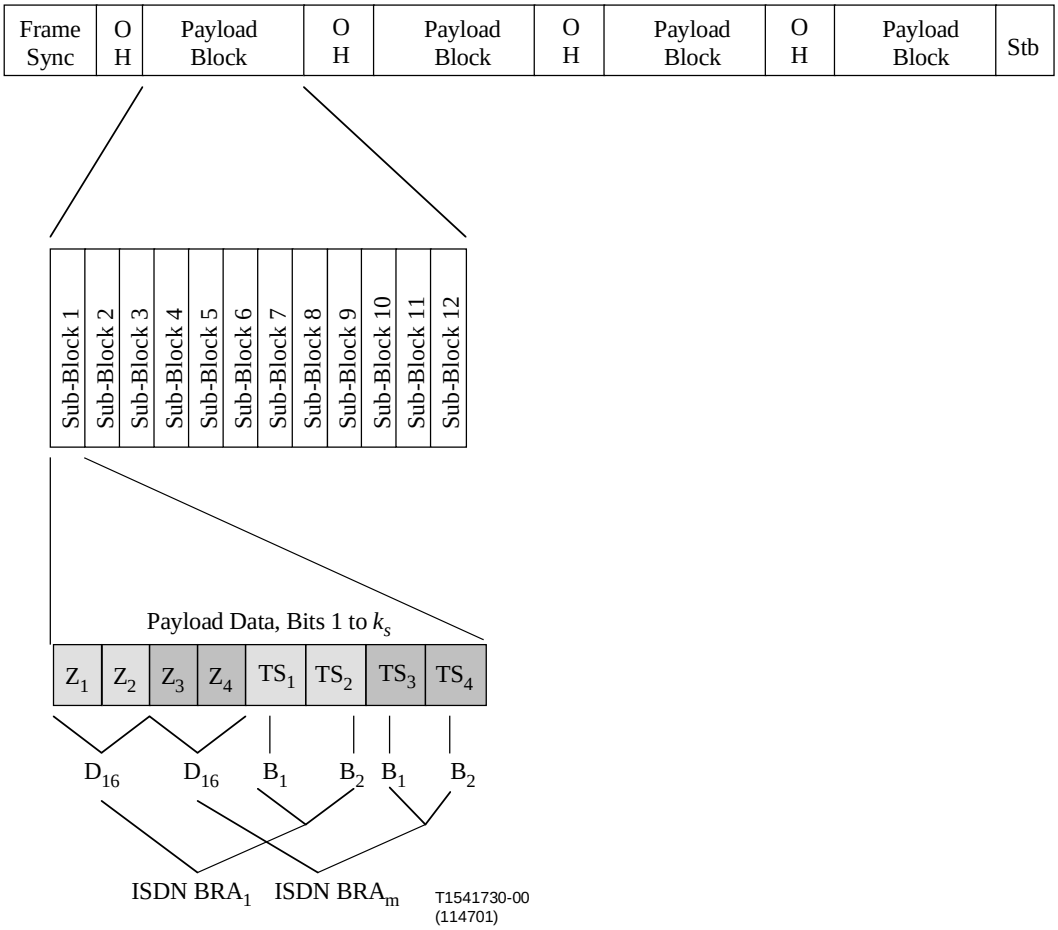


FIGURE E-8

Framing Example: 2 x ISDN BRA

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[6] If four or more ISDN BRAs are transported, four D_{16} channels are mapped on one 64 kbit/s B-channel.

The transport of the customer data channels of each ISDN BRA requires 144 kbit/s bandwidth. Table E-1 shows the number of required TS- and Z-channels.

TABLE E-1

K × ISDN BRA

Number of ISDN BRA *K*	Payload Bit Rate K×(128 kbit/s+16 kbit/s)	Application	TS-Channels (64 kbit/s) *n*	Z-Channels (8 kbit/s) *i*
1	144	1 ISDN BRA	2	2
2	288	2 ISDN BRA	4	4
3	432	3 ISDN BRA	6	6
4	576	4 ISDN BRA	9	0
5	720	5 ISDN BRA	11	2
6	864	6 ISDN BRA	13	4

E.8.4 ISDN BRA for Lifeline Service

Lifeline service in case of local power failure can be provided by one ISDN BRA. The lifeline BRA always is that one which is transported over the first time slots of each payload sub block (e.g. Z_1, Z_2, TS_1, TS_2). Remote power feeding is provided by the central office such that the transceiver can operate in a reduced power mode.

E.8.5 Time Slot Positions of ISDN B- and D_{16}-Channels (EOC Signalling)

If multiple ISDN BRAs are transported over SHDSL, certain data channels in the SHDSL payload blocks must be assigned to each ISDN BRA. Table E-2 to Table E-5 show the allocation of the ISDN data channels of up to 4 BRAs. The signalling is transmitted over the SHDSL EOC.

In order to avoid unnecessary shifting of ISDN D- and B- bits, the respective D-bits are transmitted after their B- bits in the subsequent SHDSL payload subblock (B-bits in *Nth* payload subblock and D-bits in *N*+1th payload subblock; if the B-bits are transmitted in the last payload subblock of an SHDSL frame, the D-bits are transmitted in the first payload subblock of the next SHDSL frame).

TABLE E-2

Time Slot Allocation for 1 ISDN BRA

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_1	TS_2	Z_1+Z_2

TABLE E-3

Time Slot Allocation for 2 ISDN BRAs

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_1	TS_2	Z_1+Z_2
2	TS_3	TS_4	Z_3+Z_4

TABLE E-4

Time Slot Allocation for 3 ISDN BRAs

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_1	TS_2	Z_1+Z_2
2	TS_3	TS_4	Z_3+Z_4
3	TS_5	TS_6	Z_5+Z_6

TABLE E-5

Time Slot Allocation for 4 ISDN BRAs

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_2	TS_3	TS_1 (Bit 1 and 2)
2	TS_4	TS_5	TS_1 (Bit 3 and 4)
3	TS_6	TS_7	TS_1 (Bit 5 and 6)
4	TS_8	TS_9	TS_1 (Bit 7 and 8)

E.8.5.1 Time Slot Positions of ISDN B- and D_{16}-Channels (EOC Signaling) in 4-Wire Mode

In the optional 4-wire mode, the allocation of up to 3 ISDN BRAs to Time Slots and Z-bits shall be as shown in Table E-2 to Table E-4. The allocation for 4 ISDN BRAs is shown in Table E-5A.

TABLE E-5A

Time Slot Allocation for 4 ISDN BRAs

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_1	TS_2	Z_1+Z_2
2	TS_3	TS_4	Z_3+Z_4
3	TS_5	TS_6	Z_5+Z_6
4	TS_7	TS_8	Z_7+Z_8

The Z-bits and Time Slots shall be interleaved between Pair 1 and Pair 2, such that the odd numbered Z-bits and time slots are carried on Pair 1 and the even numbered Z-bits and time slots are carried on Pair 2. See Figure E-8A for additional details.

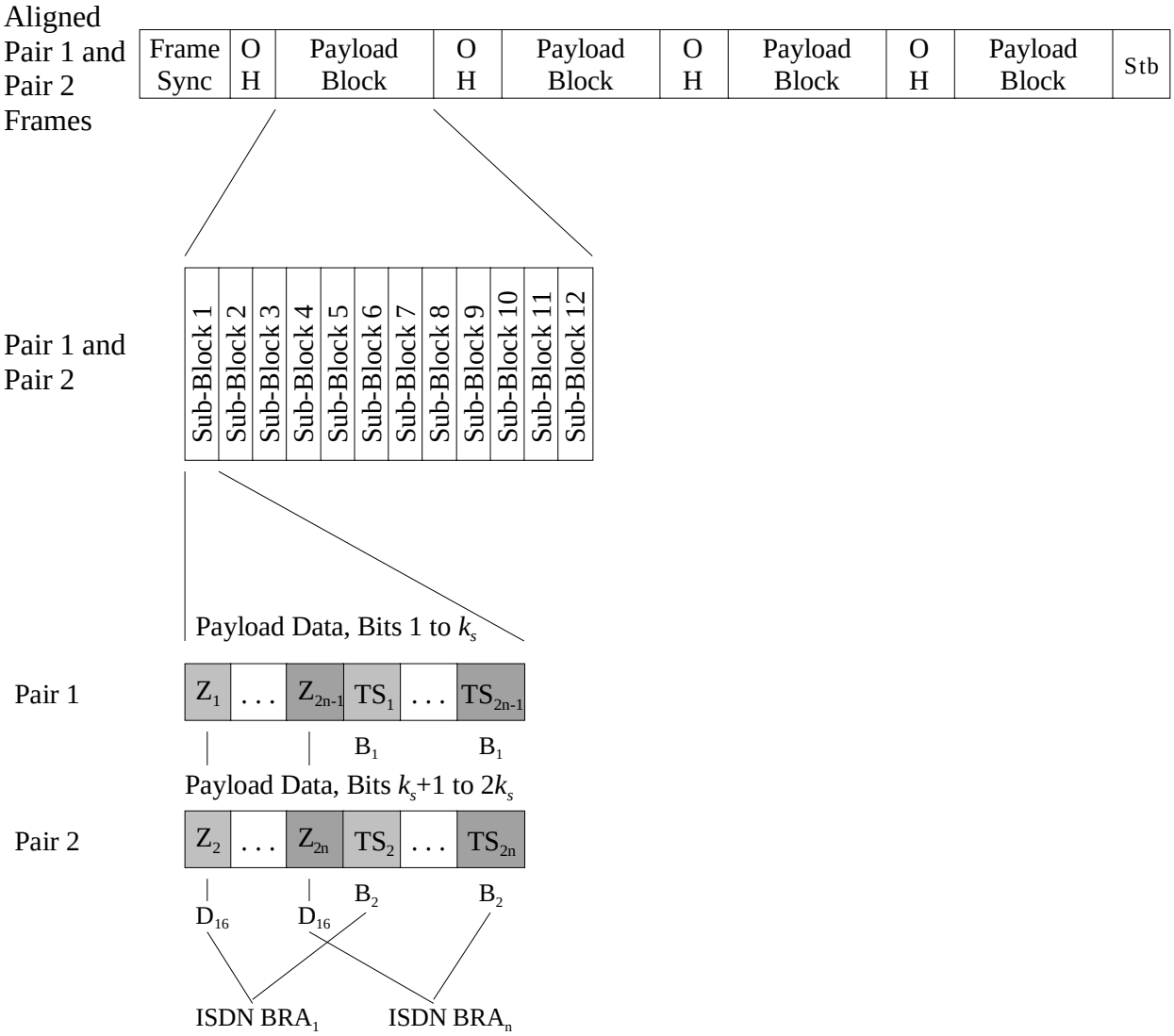

FIGURE E-8A

4-Wire Framing for ISDN BRA

E.8.6 Time Slot Positions of ISDN B- and D_{16}-Channels and the Optional Fast Signalling Channel

The optional 8 kbit/s fast signalling channel is always conveyed in Z_1, as shown in Figure E-9. If this fast signalling channel is used, up to 6 ISDN BRA can be transported over SHDSL.

In order to avoid unnecessary shifting of ISDN D- and B- bits, the respective D-bits are transmitted after their B- bits in the subsequent SHDSL payload subblock (B-bits in *Nth* payload subblock and D-bits in *N+1th* payload subblock; if the B-bits are transmitted in the last payload subblock of an SHDSL frame, the D-bits are transmitted in the first payload subblock of the next SHDSL frame).

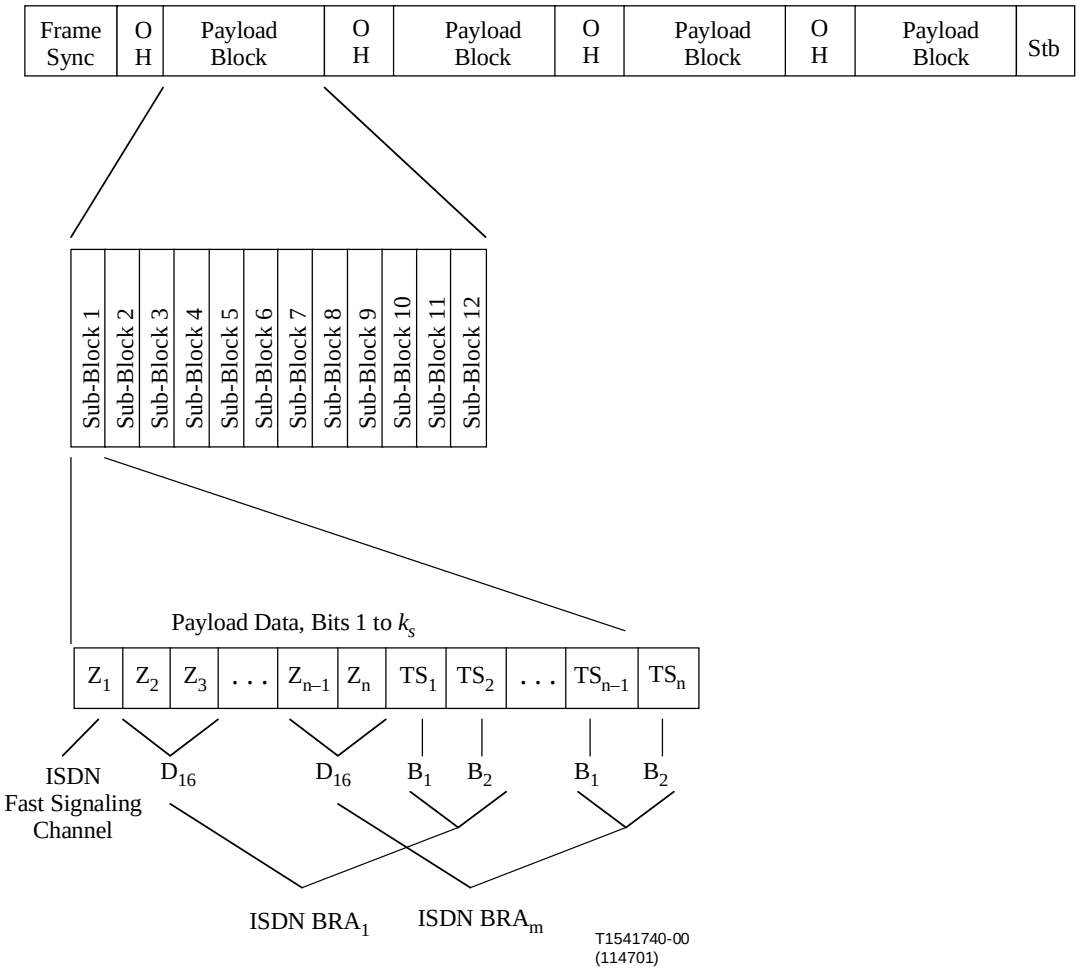

FIGURE E-9

Mapping of ISDN B- and D-Channels with a Fast Signalling Channel

TABLE E-6

Time Slot Allocation for 1 ISDN BRA using the Fast Signalling Channel

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_1	TS_2	Z_2+Z_3

TABLE E-7

Time Slot Allocation for 2 ISDN BRAs using the Fast Signalling Channel

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_1	TS_2	Z_2+Z_3
2	TS_3	TS_4	Z_4+Z_5

TABLE E-8

Time Slot Allocation for 3 ISDN BRAs using the Fast Signalling Channel

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_1	TS_2	Z_2+Z_3
2	TS_3	TS_4	Z_4+Z_5
3	TS_5	TS_6	Z_6+Z_7

TABLE E-9

Time Slot Allocation for 4 ISDN BRAs using the Fast Signalling Channel

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_2	TS_3	TS_1 (Bit 1 and 2)
2	TS_4	TS_5	TS_1 (Bit 3 and 4)
3	TS_6	TS_7	TS_1 (Bit 5 and 6)
4	TS_8	TS_9	TS_1 (Bit 7 and 8)

TABLE E-10

Time Slot Allocation for 5 ISDN BRAs using the Fast Signalling Channel

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_2	TS_3	Z_2+Z_3
2	TS_4	TS_5	TS_1 (Bit 1 and 2)
3	TS_6	TS_7	TS_1 (Bit 3 and 4)
4	TS_8	TS_9	TS_1 (Bit 5 and 6)
5	TS_{10}	TS_{11}	TS_1 (Bit 7 and 8)

TABLE E-11

Time Slot Allocation for 6 ISDN BRAs using the Fast Signalling Channel

ISDN BRA Number	ISDN B1 Time Slot	ISDN B2 Time Slot	ISDN D16 Time Slots
1	TS_2	TS_3	Z_2+Z_3
2	TS_4	TS_5	Z_4+Z_5
3	TS_6	TS_7	TS_1 (Bit 1 and 2)
4	TS_8	TS_9	TS_1 (Bit 3 and 4)
5	TS_{10}	TS_{11}	TS_1 (Bit 5 and 6)
6	TS_{12}	TS_{13}	TS_1 (Bit 7 and 8)

E.8.6.1 Time Slot Positions of ISDN B- and D_{16}-Channels (Fast Signaling) in 4-Wire Mode

In the optional 4-wire mode, the allocation of up to 3 ISDN BRAs to Time Slots and Z-bits shall be as shown in Table E-6 to Table E-8. The allocation for 4 to 6 ISDN BRAs is shown in Table E-11A to Table E-11C.

TABLE E-11A

Time Slot Allocation for 4 ISDN BRAs using the Fast Signaling Channel

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_1	TS_2	Z_2+Z_3
2	TS_3	TS_4	Z_4+Z_5
3	TS_5	TS_6	Z_6+Z_7
4	TS_7	TS_8	Z_8+Z_9

TABLE E-11B

Time Slot Allocation for 5 ISDN BRAs using the Fast Signaling Channel

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_1	TS_2	Z_2+Z_3
2	TS_3	TS_4	Z_4+Z_5
3	TS_5	TS_6	Z_6+Z_7
4	TS_7	TS_8	Z_8+Z_9
5	TS_9	TS_{10}	$Z_{10}+Z_{11}$

TABLE E-11C

Time Slot Allocation for 6 ISDN BRAs using the Fast Signaling Channel

ISDN BRA Number	ISDN B_1 Time Slot	ISDN B_2 Time Slot	ISDN D_{16} Time Slots
1	TS_1	TS_2	Z_2+Z_3
2	TS_3	TS_4	Z_4+Z_5
3	TS_5	TS_6	Z_6+Z_7
4	TS_7	TS_8	Z_8+Z_9
5	TS_9	TS_{10}	$Z_{10}+Z_{11}$
6	TS_{11}	TS_{12}	$Z_{12}+Z_{13}$

In Fast Signaling mode, the Time Slots and Z-bits frame shall be aligned within the SHDSL Payload Sub-Block such that the Z_1 Fast Signaling bit occupies the first bit position within the Payload Sub-Block on both Pair 1 and Pair 2. The remaining Z-bits and Time Slots shall be interleaved between Pair 1 and Pair 2. The even numbered Z-bits and the odd numbered time slots

are carried on Pair 1. The odd numbered Z-bits and even numbered time slots are carried on Pair 2. See Figure E-9A for additional details.

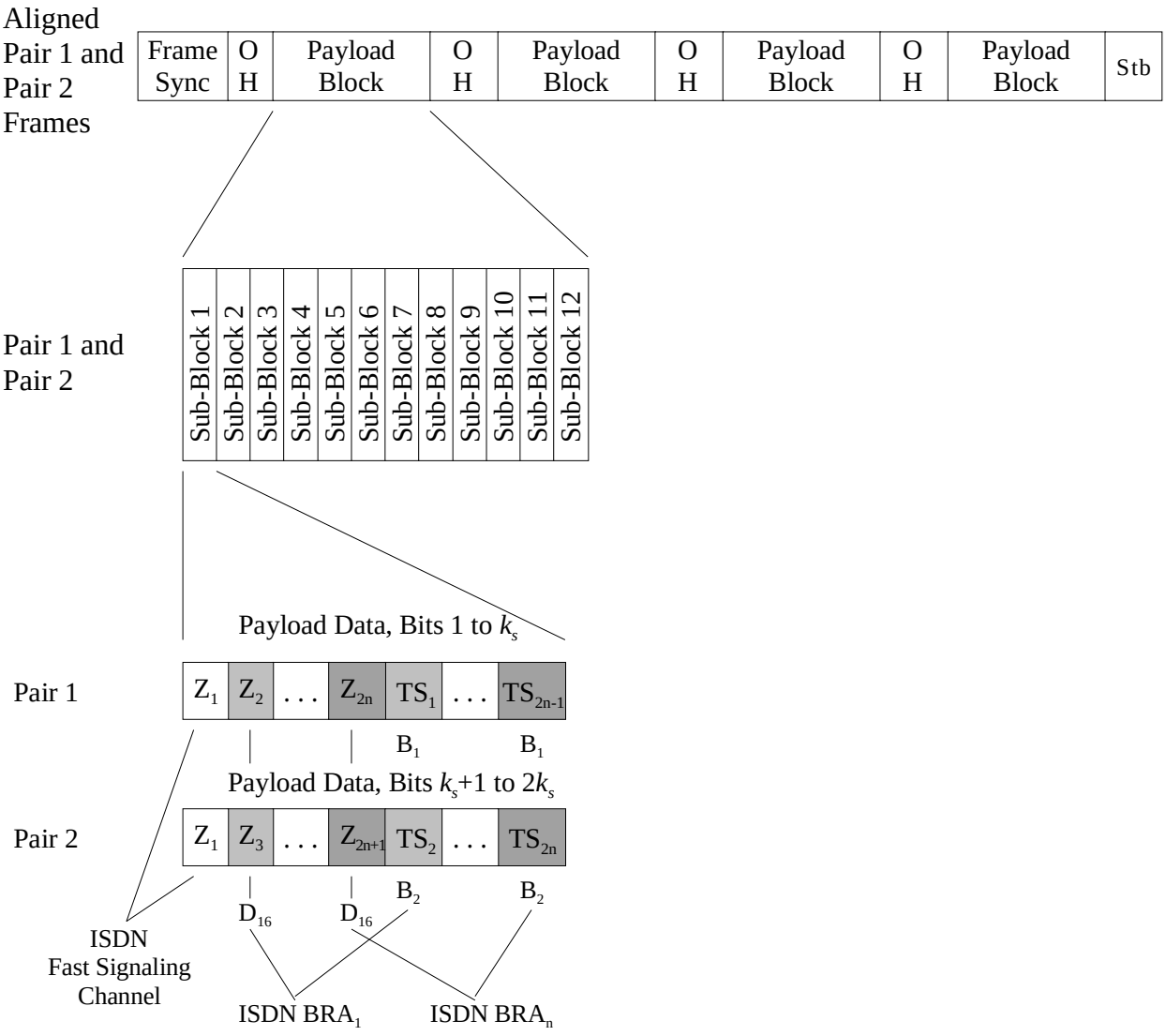

FIGURE E-9A

4-Wire Framing for ISDN BRA

E.8.7 Signalling over the SHDSL EOC or the Fast Signalling Channel

The ISDN status signalling information can be optionally transmitted over two different channels:

- SHDSL EOC
- Fast signalling channel

In both cases SHDSL EOC messages with their HDLC-like format are used to transport the ISDN message code. The STU-C as well as the STU-R unit can initiate EOC messages. Generally, the ISDN related EOC messages are transported over the SHDSL EOC. In some applications, it is necessary to set up an additional fast signalling channel with 8 kbit/s bandwidth for these ISDN

related EOC messages. This is the case when more than four ISDN BRAs are used. It may also be used when low latency signalling is required or when another TPS-TC's signalling (e.g., ATM) has substantially restricted the use of the SHDSL EOC channel.

E.8.7.1 SHDSL EOC messages

The EOC messages number 20 and 148 are used to transmit the ISDN maintenance and control functions as well as the other ISDN EOC messages.

TABLE E-12

ISDN Request – Message ID 20

Octet #	Contents	Data Type	Reference
1	Message ID 20	Message ID	
2 bits 4 – 7	ISDN BRA Number	Unsigned char	
2 bits 0 – 3	Unused		Set to 0000_2
3	ISDN message code		

TABLE E-13

ISDN Response – Message ID 148

Octet #	Contents	Data Type	Reference
1	Message ID 148	Message ID	
2 bits 4 – 7	ISDN BRA Number	Unsigned char	
2 bits 0 – 3	Unused		Set to 0000_2
3	ISDN message code		

ISDN BRA Number: Each ISDN BRA can be addressed independently. To each ISDN BRA a four digit number is assigned (BRA 1 = 0000, ... BRA 6 = 0101).

E.8.7.2 ISDN Message Codes

The message codes which are contained as an octet in the SHDSL EOC message "ISDN Requests" are listed in Table E-14. The message codes which are contained as an octet in the SHDSL EOC message "ISDN Response" are listed in Table E-15.

TABLE E-14

ISDN Message Codes Commands

Function	Message	EOC Message Code	Comment
S-Bus Control	SIA	0001 0000	S-interface activate (STU-C → STU-R)
	SID	0001 0001	S-interface deactivate (STU-C → STU-R)
	SAI	0001 0010	S-interface activated (STU-R → STU-C)
	SDI	0001 0011	S-interface deactivated (STU-R → STU-C)
ISDN Transceiver Status	ACT	0000 0001	Readiness for layer 2 communication (STU-C → STU-R) (STU-R → STU-C)
	DEA	0000 0010	Intention to deactivate (STU-C → STU-R)
	CSO	0000 0011	Cold start only (STU-R → STU-C)
BRA Termination Reset	S reset	0000 0000	Reset of ISDN control unit at STU-R (STU-C → STU-R)
ISDN EOC Messages	Operate 2B+D loopback	0011 0001	(STU-C → STU-R)
	Operate B1-channel loopback (note)	0011 0010	(STU-C → STU-R)
	Operate B2-channel loopback (note)	0011 0011	(STU-C → STU-R)
	Return to normal	0011 1111	(STU-C → STU-R)
	Hold state	0011 0000	(STU-C → STU-R)
NOTE - The use of B1 and B2 channel loopbacks is optional. However, the loopback codes are reserved for these functions.			

TABLE E-15

ISDN Message Codes Responses

Function	Message	EOC Message Code	Comment
S-Bus Control	SIA	1001 0000	S-interface activated
	SIAF	1101 0000	S-interface activation failed
	SID	1001 0001	S-interface deactivated
	SIDF	1101 0001	S-interface deactivation failed
	SAI	1001 0010	S-interface activated
	SDI	1001 0011	S-interface deactivated
ISDN Transceiver Status	ACT	1000 0001	Readiness for layer 2 communication
	DEA	1000 0010	Intention to deactivate
	CSO	1000 0011	Cold start only
BRA Termination Reset	S reset ack	1000 0000	Reset of ISDN control unit at STU-R
ISDN EOC Messages	Operate 2B+D loopback (success)	1011 0001	
	Operate 2B+D loopback (failure)	1111 0001	
	Operate B1-channel loopback (success)	1011 0010	
	Operate B1-channel loopback (failure)	1111 0010	
	Operate B2-channel loopback (success)	1011 0011	
	Operate B2-channel loopback (failure)	1111 0011	
	Return to normal (success)	1011 1111	
	Return to normal (failure)	1111 1111	
	Hold state	1011 0000	
	Unable to comply acknowledgement	1111 0100	

E.8.8 S-Bus Control

The ISDN S-buses which connect the ISDN terminals with the STU-R can be controlled independently with the respective message codes (SIA, SID, SAI, SDI) for each S-bus. The STU-C side can activate and deactivate the S bus and gets status information. These messages are transmitted as SHDSL EOC messages.

The S-interfaces of each ISDN BRA can be addressed independently. To each ISDN BRA a four digit number is (BRA 1 = 0000, ... BRA 6 = 0101) contained in the ISDN related SHDSL EOC messages.

SIA: In STU-C to STU-R direction this function is used to request the STU-R to activate the interface at the S reference point. If the interface at the S reference point is to be activated this message may be sent. In STU-R to STU-C direction the respective responses are SIA (S-interface activated) or SIAF (S-interface activation failed).

SID: In STU-C to STU-R direction this function is used to request the STU-R to deactivate the interface at the S reference point. If the interface at the S reference point is to be deactivated this message may be sent. In STU-R to STU-C direction the respective responses are SID (S-interface deactivated) or SIDF (S-interface deactivation failed).

SAI: In STU-R to STU-C direction this message is used to inform the STU-C, that the S-interface and S-bus have been activated.

SDI: In STU-R to STU-C direction this message is used to inform the STU-C, that the S-interface and S-bus have been deactivated.

TABLE E-16

Flowchart: S Interface

STU-C: activate S-interface command	EOC S act (SIA) →	STU-R: activate and send result
	← EOC S act ackn (SIA/SIAF)	
STU-C: deactivate S-interface command	EOC S deact (SID)→	STU-R: deactivate and send result
	← EOC S deact ackn (SID/SIDF)	
STU-C: acknowledge	← EOC S ActInd (SAI)	STU-R: indicate activation
	EOC S ActInd ackn (SAI)→	
STU-C: acknowledge	← EOC S DeactInd (SDI)	STU-R: indicate deactivation
	EOC S DeactInd ackn (SDI)→	

E.8.9 BRA Termination Reset

The status and condition of each ISDN BRA and its S-interface at the STU-R side can be individually monitored from the STU-C side. If a failure or blocking at one ISDN BRA is detected this situation can be resolved by a reset. "BRA termination reset" puts the control unit of the S-interface to its default state (the deactivated state). Other BRAs or other services are not affected.

TABLE E-17

Reset Request

Message	EOC Message Code	Comment
S reset	0000 0000	

TABLE E-18

Reset Response

Message	EOC Message Code	Comment
S reset acknowledge	1000 0000	

E.8.10 Transport of ISDN EOC messages over SHDSL EOC

Table E-19 shows the six of the eight codes of the EOC functions which are defined in the ISDN standard. (The two messages concerning the corrupted CRC are not required).

TABLE E-19

ISDN EOC Message Codes

Origin (o) & destination (d) & transfer (t)				
Message	Message code	Network	STU-R1	REG
Operate 2B+D loopback	0011 0001	O	d	t/d
Operate B1-channel loopback (note)	0011 0010	O	d	t/d
Operate B2-channel loopback (note)	0011 0011	O	d	t/d
Return to normal	0011 1111	O	d	t/d
Hold state	0011 0000	d/o	o/d	o/d/t
NOTE - The use of B1 and B2 channel loopbacks is optional. However, the loopback codes are reserved for these functions.				

E.9 TPS-TC for ATM Transport

E.9.1 Definitions

ATM Asynchronous Transfer Mode

HEC Header Error Check

E.9.2 Reference Model for ATM Transport

The ATM TC layer for SHDSL is consistent with ITU-T Recommendation I.432.1 [8]. It shall provide the following functions, as defined in ITU-T I.432.1:

- Rate decoupling between ATM layer and the synchronous (or plesiochronous) PMS-TC layer.

- Insertion/Extraction[4] of Idle cells.
- Insertion/Extraction[5] of ATM Header Error Check (HEC) byte.
- Cell payload scrambling / descrambling for SDH-based systems.
- Cell delineation in the receive channel.
- Bit timing and ordering (MSB sent first with bit timing synchronous to the STU-C downstream timing base).

The HEC covers the entire cell header. The code used for this function is capable of either:

- single bit error correction or
- multiple bit error detection.

Error detection shall be implemented as defined in ITU-T Recommendation I.432.1[8] with the exception that any HEC error shall be considered as a multiple bit error, and therefore, HEC error correction shall not be performed.

Figure E-10 shows the logical interface between the ATM Layer, the ATM-TC and the SHDSL PMS-TC function.

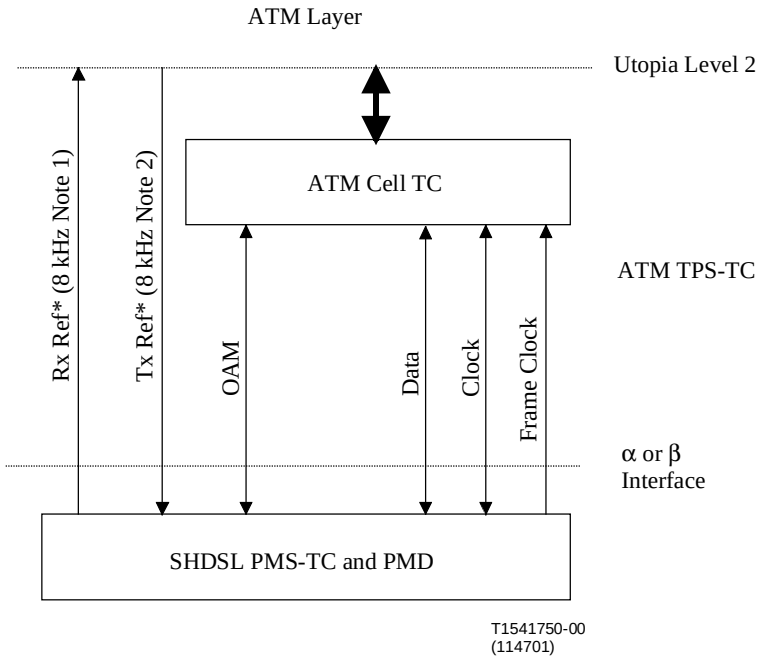

FIGURE E-10

ATM -TC Logical Interface to PMS-TC and TPS-TC ATM Layer

NOTE 1 - RxRef may be present at the STU-R.

NOTE 2 - TxRef may be present at the STU-C.

An ATM Utopia level 2 interface connects the ATM-TC to the ATM Layer. This interface may also be realized logically. Byte boundaries, at the ATM Utopia interface, shall be preserved in the

---

[4] An idle cell inserted at the transmit side has to be extracted at the remote side.

[5] A HEC byte inserted at the transmit side has to be extracted at the remote side.

SHDSL payload. Bytes are transmitted MSB first, in accordance with ITU-T recommendation I.432.1 [8].

E.9.2.1 Framing

The PMS-TC provides a clear channel to the ATM-TC and cells are mapped into the SHDSL payload on a byte by byte basis. At the STU-C, cells are mapped across the logical α interface while at the STU-R, cells cross the logical β interface, as identified in § 4.1. At the α and β interface, logical data and clock lines are present. Cell alignment to the frame is optional. The ATM stream shall be aligned within the SHDSL Payload Sub-Block such that the byte boundaries are preserved. Each Payload Sub-Block is treated as containing *n* 8-bit time slots. Each byte from the input ATM data stream is mapped MSB-first into the next available time slot. The first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, …, time slot *n*. k_s bits (or *n* bytes) of contiguous data shall be contained within each Sub-Block, as specified in § 8.1. $k_s = i + n \times 8$, and, in this mode, $i = 0$ and $3 \leq n < 36$. See Figure E-10A for additional details.

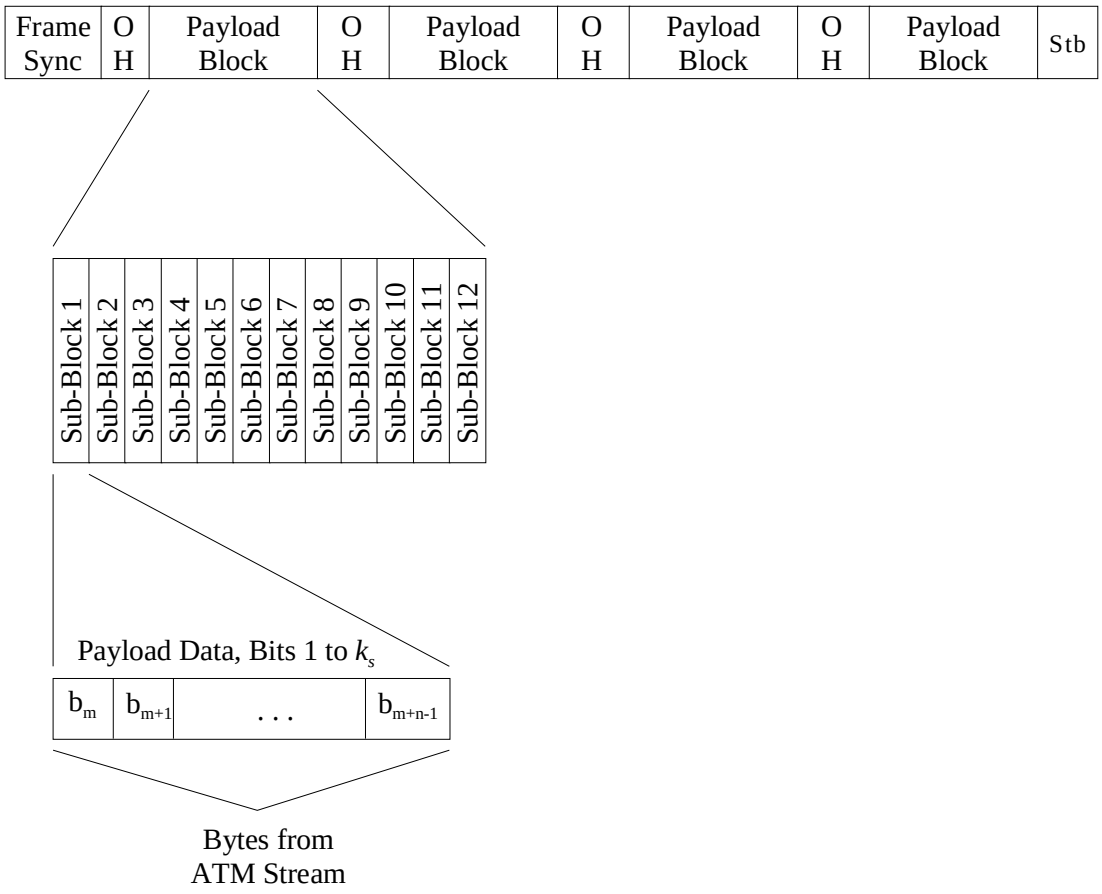

FIGURE E-10A

ATM Framing

In the optional 4-wire mode, ATM data is carried over both pairs using interleaving, as described in § 8.2. A total of $2k_s$ bits ($2n$ bytes) of byte-oriented data shall be transported per SHDSL Payload Sub-Block. $k_s = i + n\times 8$, and, in this mode, $i = 0$ and $3 \le n \le 36$. Only even numbers of time slots are supported in 4-wire mode. The input ATM stream shall be aligned within the SHDSL Payload Sub-Block such that the byte boundaries are preserved. Each Payload Sub-Block is treated as containing $2n$ 8-bit time slots. Each byte from the input ATM data stream is mapped MSB-first into the next available time slot. The first time slot begins at the first bit position within the Payload Sub-Block, followed by time slot 2, time slot 3, …, time slot n. $2k_s$ bits (or $2n$ bytes) of contiguous data shall be contained within each Sub-Block, as specified in §8.1. $k_s = i + n\times 8$, and, in this mode, $i = 0$ and $3 \le n < 36$. The bytes from the input ATM data stream shall be interleaved between Pair 1 and Pair 2, such, where byte b_m is carried on Pair 1, byte b_{m+1} is carried in the corresponding time slot on Pair 2. See Figure E-10B for additional details.

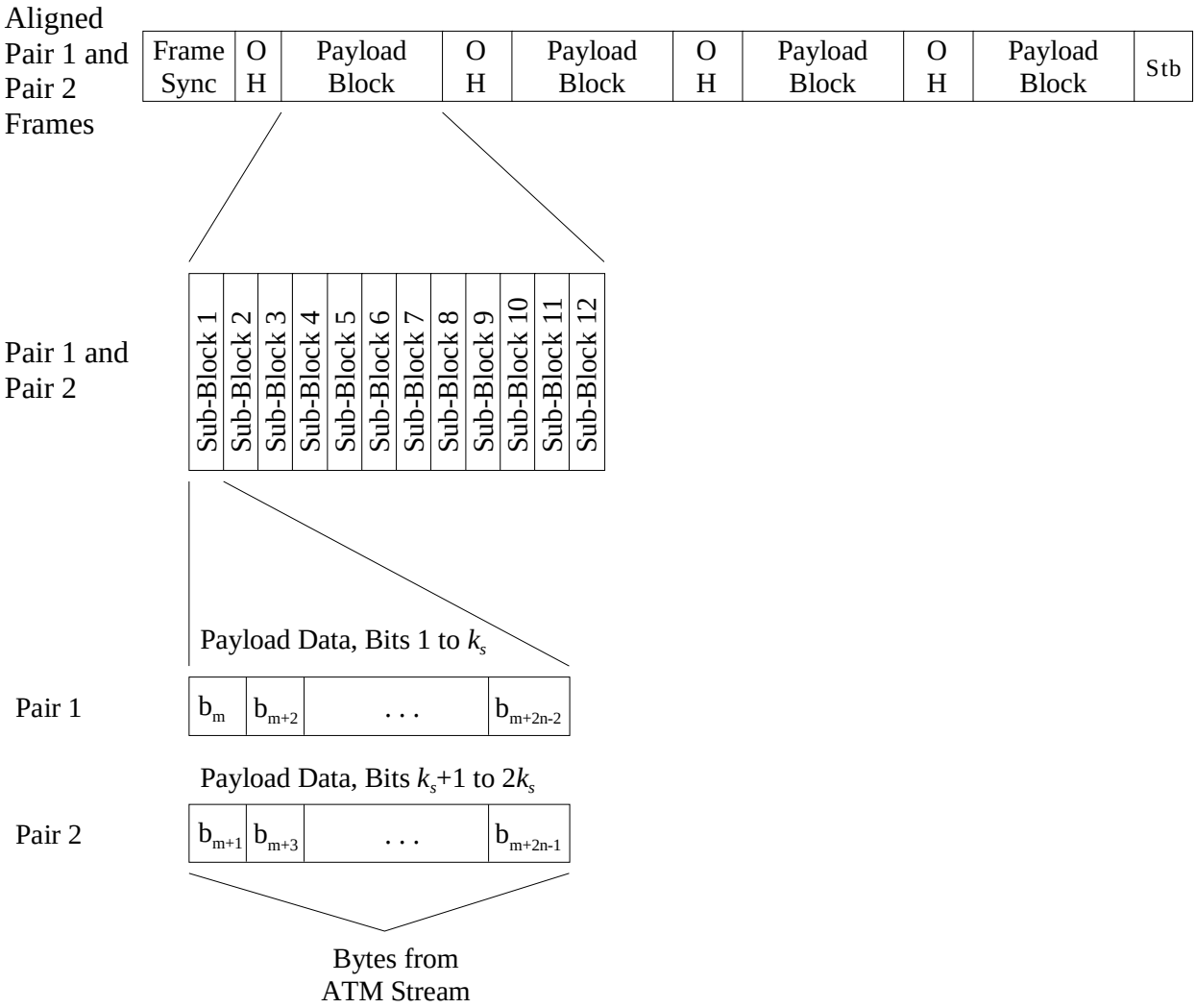

FIGURE E-10B

4-Wire Framing for ATM

E.9.2.2 Timing

STUs shall be operated in either synchronous or plesiochronous mode; however, in most applications synchronous operation is preferred. In either case, the STU-C frame clock is locked to network timing.

The provision of Network Timing Reference from the STU-C to the STU-R for ATM is optional; however, if an NTR is provided, the SHDSL PMS-TC shall operate in clock synchronization mode 3a (see § 10.1). The network timing reference shall be an 8 kHz marker from which clocks at other frequencies could easily be derived. In this clock mode, both the frame and symbol clocks at the STU-C are locked to the NTR. The STU-R may extract the NTR from the received Frame Synchronization Word (FSW). Referring to Figure E-10, the TxRef (in the STU-C) lines carries NTR directly to the PMS-TC, while RxRef (in the STU-R) carries the NTR to the ATM Layer from PMS-TC. Synchronization to the NTR shall be as described in § 10.4.

E.9.3 Transport Capacity and Flow Control

An STU transporting ATM shall support N x 64 kbit/s data rates. The payload data rate shall be: $n\times64 + i\times8$ kbit/s, where $3 \le n \le 36$ and $i = 0$. This restriction applies to the data rate and payload block size, as specified in § 7.1.1, § 8.1, and § 8.2.

In the optional four-wire mode, the rates specified shall apply per pair.

The ATM-TC shall provide flow control, allowing the STU-C and STU-R to control the cell flow from the ATM layer. This functionality is implemented through the TX_Cell Handshake and RX_Cell handshake at the ATM Utopia bus interface. A cell may be transferred to the ATM-TC layer only after the completion of a TX_Cell Handshake. Similarly, a cell may be transferred from the ATM-TC to the ATM Layer only after the STU has completed an RX_Cell_Handshake. This functionality is important to avoid cell overflow and underflow at the TU layer.

E.9.4 Operations and Maintenance

The ATM-TC requires Operation and Maintenance (OAM) functionality. The messaging protocol and format should be handled in accordance with § 9. The OAM functions notify the OAM entity at the opposite end of the line upon the status of the cell delineation process (e.g. Header Error Check (HEC) anomalies and Loss of Cell Delineation defects (LCD)). Performance parameters are derived from anomalies and defects.

E.9.4.1 ATM Data Path Related Near-End Anomalies

Near-end No Cell Delineation (nncd) anomaly: An *nncd* anomaly occurs immediately after ATM-TC start-up, when ATM data is received and the cell delineation process is in HUNT or PRESYNC state. Once cell delineation is acquired, subsequent losses of cell delineation shall be considered *nocd* anomalies.

Near-end Out of Cell Delineation (nocd) anomaly: An *nocd* anomaly occurs when the cell delineation process in operation transitions from the SYNC state to HUNT state. An *nocd* anomaly terminates when the cell delineation process transition from PRESYNC to SYNC state or when *nlcd* defect maintenance status is entered.

Near-end Header Error Control (nhec) anomaly: An *nhec* anomaly occurs when an ATM cell header error control fails.

E.9.4.2 ATM Data Path Related Near-End Defects

Near-end Loss of Cell Delineation (nlcd) defect: An *nlcd* defect occurs when at least one *nocd* is present in 9 consecutive SDSL frames and no *losw* defect (loss of synchronization word) is detected.

E.9.4.3 ATM Data Path Related Far-End Anomalies

Far-end No Cell Delineation (fncd) anomaly: An *fncd* anomaly is an *nncd* anomaly that is reported from the far end by the NCD indicator in the EOC ATM Cell Status Information message. An *fncd* anomaly occurs immediately after start-up and terminates if the received NCD indicator is coded 0.

Note that, since the far-end reports the NCD indicator only on request, the *fncd* anomaly may be inaccurate for derivation of the far-end NCD failure. Therefore, the NCD failure is autonomously reported from the far-end.

Far-end Out of Cell Delineation (focd) anomaly: A *focd* anomaly is a *nocd* anomaly, that is reported from the far end by the OCD indicator in the EOC ATM Cell Status Information message. The OCD indicator shall be coded 0 to indicate no *nocd* anomaly has occurred since last reporting and shall be coded 1 to indicate that at least one *nocd* anomaly has occurred since last reporting. An *focd* anomaly occurs if no *fncd* anomaly is present and a received OCD indicator is coded 1. An *focd* anomaly terminates if a received OCD indicator is coded 0.

Far-end Header Error Control (fhec) anomaly: An *fhec* anomaly is an *nhec* anomaly, that is reported from the far end by the HEC indicator in the EOC ATM Cell Status Information message. The HEC indicator shall be coded 0 to indicate no *nhec* anomaly has occurred since last reporting and shall be coded 1 to indicate that at least one *nhec* anomaly has occurred since last reporting. An *fhec* anomaly occurs if a received HEC indicator is coded 1. An *fhec* anomaly terminates if a received HEC indicator is coded 0.

E.9.4.4 ATM Data Path Related Far-End Defects

Far-end Loss of Cell Delineation: (flcd) defect: An *flcd* defect is an *nlcd* that is reported from the far end of the line by the LCD indicator in the EOC ATM Cell Status Information message. The LCD indicator shall be coded 0 to indicate no *nlcd* defect has occurred since last reporting and shall be coded 1 to indicate that at least one *nlcd* defect has occurred since last reporting. An *flcd* defect occurs when the LCD indicator is coded 1. An *flcd* defect terminates when the LCD indicator is coded 0.

Note that, since the far-end reports the LCD indicator only on request, the *flcd* defect may be inaccurate for derivation of the far-end LCD failure. Therefore, the LCD failure is autonomously reported from the far-end.

E.9.4.5 ATM Cell Level Protocol Performance Information Collection

HEC violation count (hvc): An *hvc* performance parameter is the count of the number of *nhec* anomalies modulo 65536.

HEC total count (htc): An *htc* performance parameter is the count of the total number of cells passed through the cell delineation process, while operating in the SYNC state, since the last reporting.

These values shall be counted, such that the Management system is able to retrieve current counts on a 15-minutes and 24-hours basis.

E.9.4.6 Failures and Performance Parameters

nncd failures and *nlcd* failures relate to persistent *nncd* anomalies and persistent *nlcd* defects, respectively. The definitions below are derived from ITU-T Recommendation G.997.1 §7.1.2 [3]. These failures are reported in the ATM Cell Status Information message.

E.9.4.6.1 ATM Data Path Related Near-End Failures

The following near-end failure indications shall be provided by the STU-C and the STU-R:

E.9.4.6.1.1 Near-End No Cell Delineation (*nncd*) Failure

An *nncd* failure is declared when an *nncd* anomaly persists for more than 2.5 ± 0.5 s after the start of Data Mode. An *nncd* failure terminates when no *nncd* anomaly is present for more than 10 ± 0.5 s.

E.9.4.6.1.2 Near-End Loss of Cell Delineation (*nlcd*) failure

An *nlcd* failure is declared when an *nlcd* defect persists for more than 2.5 ± 0.5 s. An *nlcd* failure terminates when no *nlcd* defect is present for more than 10 ± 0.5 s.

E.9.4.6.2 ATM Data Path Related Far-End Failures

The following far-end failure indications shall be provided at the STU-C (the STU-R is at the far-end), and are optional at the STU-R (the STU-C is at the far-end).

E.9.4.6.2.1 Far-End No Cell Delineation (*fncd*) Failure

An *fncd* failure is declared when an *fncd* anomaly persists for more than 2.5 ± 0.5 s after the start of Data Mode. An *fncd* failure terminates when no *fncd* anomaly is present for more than 10 ± 0.5 s.

E.9.4.6.2.2 Far-End Loss of Cell Delineation (*flcd*) Failure

An *flcd* failure is declared when an *flcd* defect persists for more than 2.5 ± 0.5 s. An *flcd* failure terminates when no *flcd* defect is present for more than 10 ± 0.5 s.

E.9.4.7 EOC ATM Cell Status Request Message Format – Message ID 17

The ATM Cell Status Request/Confirmation message is used for two purposes. This message is used as ATM Cell Status Request message to get the STU-R ATM Status. For this purpose the whole information of EOC ATM Cell Status Information message - Message ID 145 shall be sent in response to this message. If an unexpected receipt of ATM Cell Status message, Message ID 145 is received including NCD or LCD failure indication, this message may be used to confirm the reception and stop future autonomous transmission of the ATM Cell Status message, Message ID 145 due to the current failure condition.

TABLE E-20

ATM Cell Status Request Information Field

Octet #	Information Field	Data Type
1	Message ID 17	Message ID

E.9.4.8 EOC ATM Cell Status Information Message Format – Message ID 145

The ATM Cell Status Information message shall be sent in response to the ATM Cell Status Request message and shall be sent autonomously upon the occurrence of an *nlcd* Failure or an *nncd* Failure. Table E-21 shows the OAM message bit encoding for an ATM Cell Status Information message. The HEC Indicator is implicitly defined as set to 1 if the HEC violation count has changed since last reporting and set to 0 otherwise. If sent autonomously, Message ID 145 is sent once every second until a Message ID 17 is received from the STU-C or the failure is cleared.

The NCD, OCD, and LCD Indicator bits shall indicate the state of *nncd* anomaly, *nocd* anomaly, and *nlcd* defect, respectively. NCD Failure and LCD Failure bits shall serve as indications of *nncd* failure and *nlcd* failure, respectively.

TABLE E-21

ATM Cell Status Information message

Octet #	Contents	Data Type	Reference
1	Message ID 145	Message ID	
2, bit 7	NCD Indicator (see NOTE)	Bit	0 = OK, 1 = alarm
2, bit 6	OCD Indicator (see NOTE)	Bit	0 = OK, 1 = alarm
2, bit 5	LCD Indicator (see NOTE)	Bit	0 = OK, 1 = alarm
2, bit 4-2	Reserved		
2, bit 1	NCD Failure	Bit	0 = OK, 1 = alarm
2, bit 0	LCD Failure	Bit	0 = OK, 1 = alarm
3	HEC violation count (*hvc*)	MS Byte	16-bit counter, modulo 65536
4	HEC violation count (*hvc*)	LS Byte	16-bit counter, modulo 65536
NOTE - Only one of the NCD, OCD, and LCD Indicators can be set to 1 at any time.			

E.10 Dual Bearer TPS-TC Mode

The TPS-TC modes in § E.1 through § E.9 are described as operating in Single-Bearer Mode; i.e., the payload is treated as a single data stream, and the TPS-TC uses all of the bits in each Payload Sub-Block. In some applications, however, it is desirable to split the payload into separate data streams supporting multiple user interfaces or different data types. Dual-Bearer Mode provides support for these cases.

Support for Dual-Bearer Mode is optional, as is support for each of the Dual-Bearer TPS-TC combinations specified in Table E-22.

In Dual-Bearer Mode, each Payload Sub-Block is split between two separate TPS-TC instances. The TPS-TC modes are negotiated independently in G.994.1, and there is no direct interaction between them. TPS-TC_a is assigned the first k_{sa} bits of each Payload Sub-Block, and TPS-TC_b is assigned the last k_{sb} bits of each Payload Sub-Block (see Figure E-11). For each of the two TPS-TCs, the k_s bits assigned to it are treated as if they constituted a complete Payload Sub-Block, and appropriate framing is applied, as described in the paragraph (§ E.1 to § E.9) associated with the selected TPS-TC.

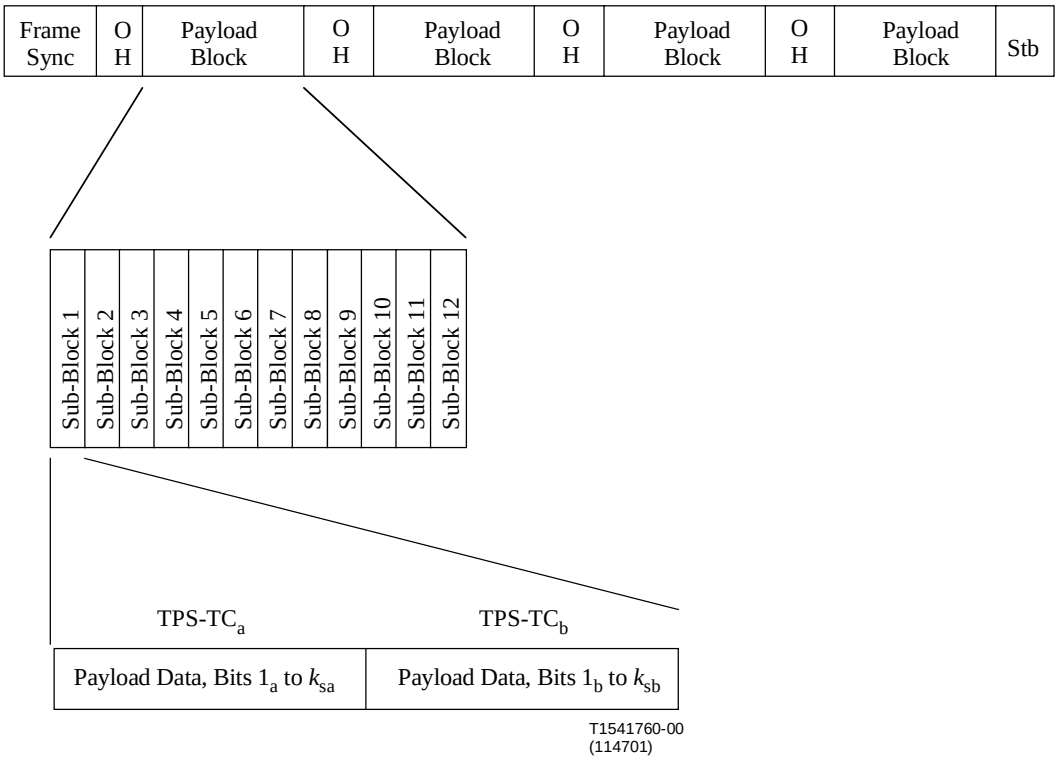

FIGURE E-11

Dual-Bearer Mode TPS-TS Framing

Figure E-12 shows an example of a Dual-Bearer mode in which Fractional DS1 is TPS-TC_a and ATM is TPS-TC_b.

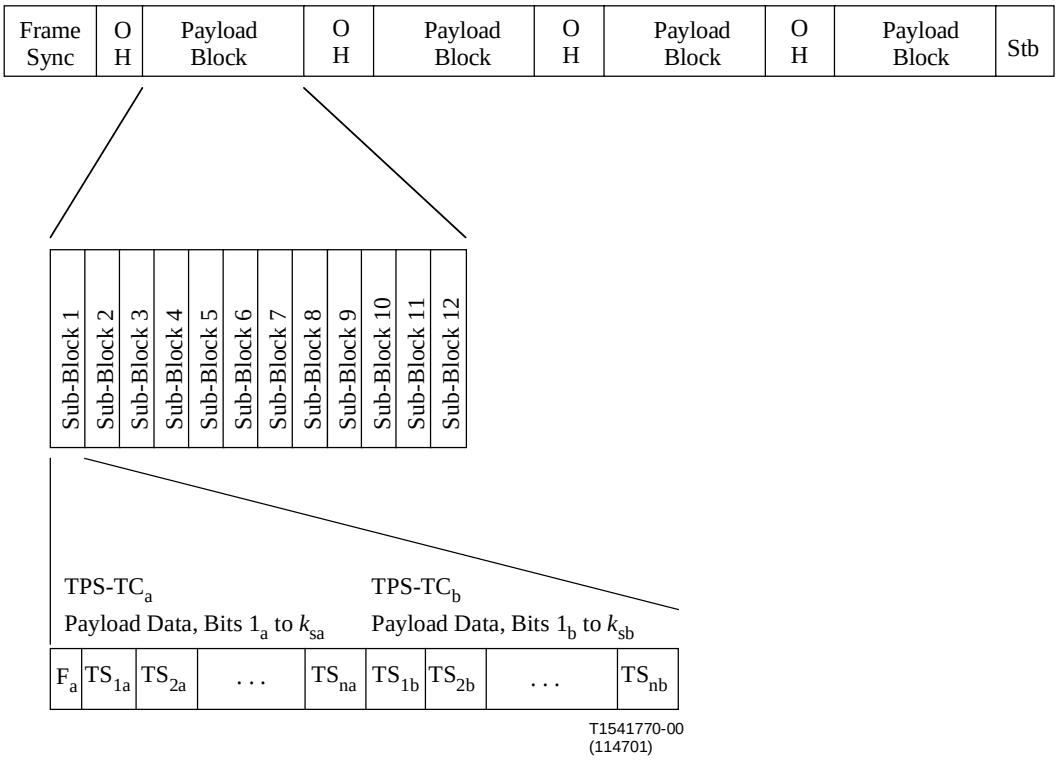

FIGURE E-12

Example of Dual-Bearer Mode TPS-TS Framing

In the optional four-wire mode, the same procedure is followed for Dual-Bearer Mode. The first k_{sa} bits on each pair are assigned to TPS-TC_a, and the last k_{sb} bits on each pair are assigned to TPS-TC_b. The appropriate four-wire TPS-TC framing is then applied, as described in § E.1 through § E.9.

E.10.1 Dual Bearer Clock Synchronization

In Dual-Bearer Mode, it is assumed that timing for the two Bearer Channels is derived from a common source and that the two data streams thus have a definite clocking relationship. As such, no mechanism is provided within the payload blocks to maintain synchronization between the Bearer Channels, regardless of the clock mode that is selected (§ 10.1).

Note that some TPS-TCs have limitations on the clock modes that are supported. Specifically, ATM using NTR (§ E.9.2) and Synchronous ISDN BRA (§ E.8) are only defined for Clock Mode 3a (see § 10.1). When either of these TPS-TCs is used as part of a Dual-Bearer Mode, the system shall operate in Clock Mode 3a.

E.10.2 Dual Bearer Mode Types

The following three types of dual bearer modes are supported within SHDSL:

Type 1 - Synchronous ISDN BRA + Broadband

Type 2 - Narrow-band + ATM

Type 3 - Narrow-band + Clear Channel

For each type of dual bearer mode, separate specification bits are provided within G.994.1 for the selection of the two TPS-TCs to be used. Table E-22 lists the combinations that are supported. Other supported types are for further study.

TABLE E-22

Supported TPS-TCs in Dual Bearer Mode

Type	**Description**	**TPS-TC$_a$**	**TPS-TC$_b$**
1	Synchronous ISDN BRA + Broadband	Synchronous ISDN BRA (§ E.8)	Clear Channel (§ E.1) Clear Channel Byte-Oriented (§ E.2) Unaligned DS1 (§ E.3) [1] Aligned DS1/Fractional DS1 (§ E.4) [1] Unaligned D2048U (§ E.5) [2] Unaligned D2048S (§ E.6) [2] Aligned D2048S/Fractional D2048S (§ E.7) [2] ATM (§ E.9)
2	Narrow-band + ATM	Unaligned DS1 (§ E.3) [1] Aligned DS1/Fractional DS1 (§ E.4) [1] Unaligned D2048U (§ E.5) [2] Unaligned D2048S (§ E.6) [2] Aligned D2048S/Fractional D2048S (§ E.7) [2]	ATM (§ E.9)
3	Narrow-band + Clear Channel	Unaligned DS1 (§ E.3) [1] Aligned DS1 / Fractional DS1 (§ E.4) [1] Unaligned D2048U (§ E.5) [2] Unaligned D2048S (§ E.6) [2] Aligned D2048S/Fractional D2048S (§ E.7) [2]	Clear Channel (§ E.1) Clear Channel Byte-Oriented (§ E.2)
NOTES: [1] denotes TPS-TC modes that typically apply only in North American networks [2] denotes TPS-TC modes that typically apply only in European networks			

APPENDIX I

Test Circuit Examples (Informative)

I.1 Example Crosstalk injection test circuit

The following is an example of a high-impedance crosstalk injection circuit.

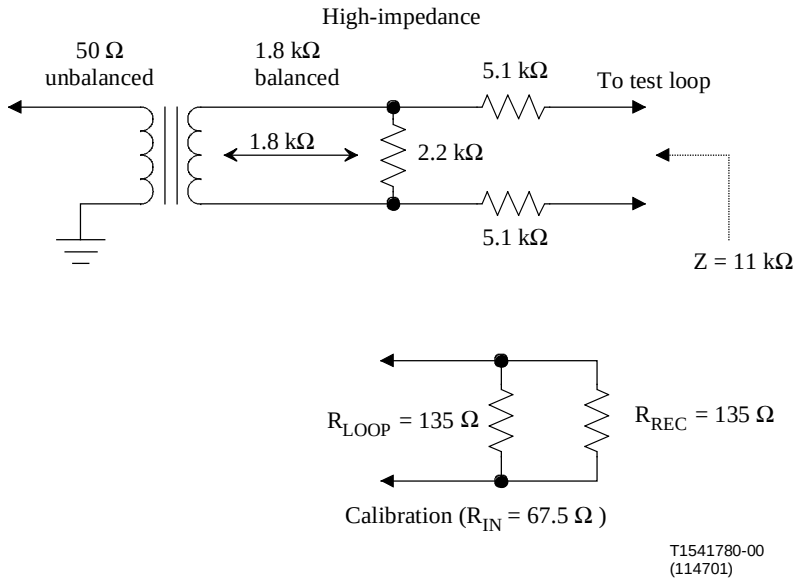

FIGURE I-1

Example high-impedance crosstalk injection circuit

I.2 Example Coupling Circuits for Longitudinal Balance and Longitudinal Output Voltage

Longitudinal balance and longitudinal output voltage may be measured using the coupling circuits described in ANSI/IEEE Std 455-1985 [B7] and ITU-T Recommendation O.9 [B8]. The coupling circuit in Figure I-2 is based upon the measurement method defined in ANSI/IEEE Std 455-1985. In order to provide sufficient measurement resolution the resistors must be matched within 0.05 % tolerance. The coupling circuit in Figure I-3 is based on the measurement method described in ITU-T Recommendation O.9. This test circuit uses precision balanced (bifilar wound) transformers/baluns and does not require precision matched resistors. The balun circuit is often more convenient for high-frequency measurements.

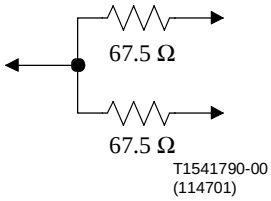

FIGURE I-2

Example Resistive Coupling Circuit

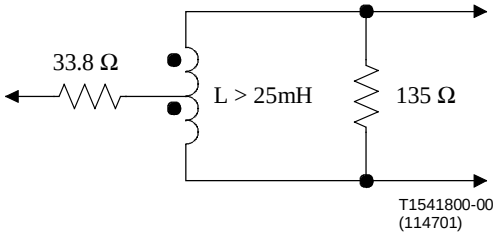

FIGURE I-3

Example Balun Coupling Circuit

I.3 Return loss test circuit

The test circuit in Figure I-4 is based upon the traditional return loss bridge with added components to accommodate the DC power feed voltage and provide transformer isolation for the measurement instrumentation. Transformer isolation of both test signal source and meter load prevent measurement errors from unintentional circuit paths through the common ground of the instrumentation and the DUT power feed circuitry. Input V_{IN} is connected to a sweeping sine wave generator (50 Ω source) and V_{OUT} is connected to a high-impedance frequency selective voltmeter (or spectrum analyser). For this test circuit the return loss is defined as follows:

$$\text{Return Loss}(f) = 20\log\left|\frac{Z_{TEST}(f) + Z_{REF}}{Z_{TEST}(f) - Z_{REF}}\right|$$

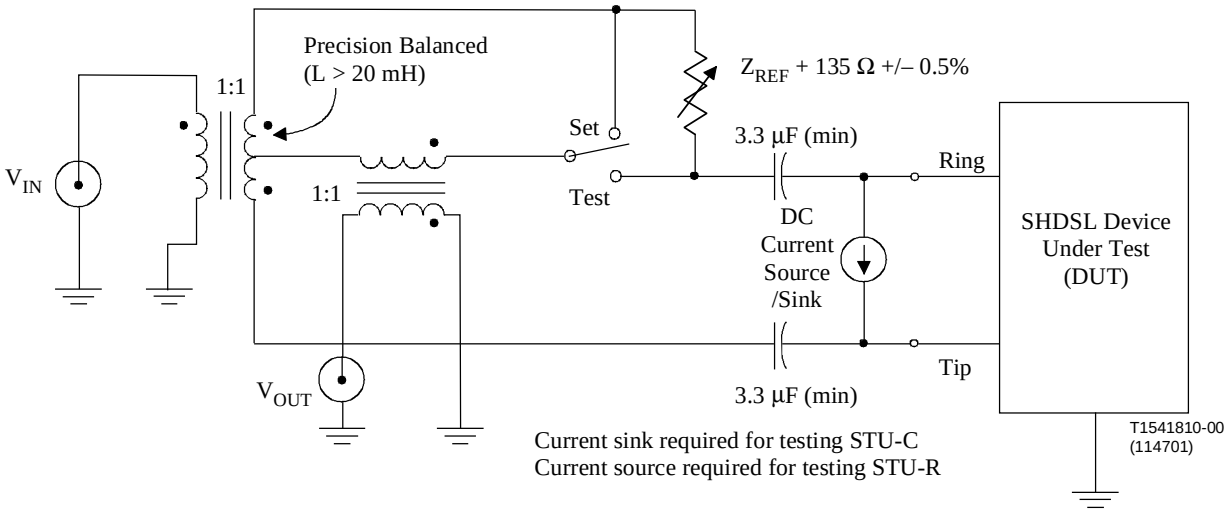

FIGURE I-4

Example return loss bridge test circuit (ground isolated)

I.4 Transmit PSD/total power measurement test circuit

The test circuit in Figure I-5 is designed to measure total transmit power and transmit PSD. The test contains provisions for DC power feed and transformer isolation for the measurement instrumentation. Transformer isolation of the instrumentation input prevents measurement errors from unintentional circuit paths through the common ground of the instrumentation and the DUT power feed circuitry. V_{OUT} is connected to a high-impedance wideband rms voltmeter (or spectrum analyser).

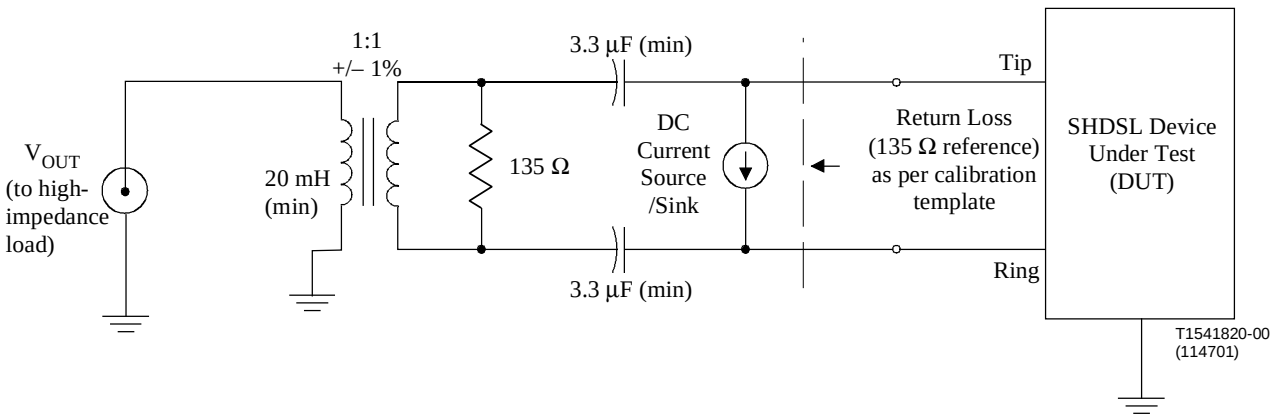

FIGURE I-5

Example ground-isolated power/PSD measurement test circuit

APPENDIX II

Typical Characteristics of Cables (Informative)

II.1 Typical Characteristics of Cables for Annex B

NOTE - For all the tables in this Appendix, the value of G' is negligible and assumed to be 0.

TABLE II.1

Parameters of PE 04

Frequency	**0 Hz**	**10 kHz**	**20 kHz**	**40 kHz**	**100 kHz**	**150 kHz**	**200 kHz**	**400 kHz**	**500 kHz**
R' (Ω/km)	268	268	269	271	282	295	312	390	425
L' (µH/km)	680	678	675	669	650	642	635	619	608
C' (nF/km)	45.5	45.5	45.5	45.5	45.5	45.5	45.5	45.5	45.5

TABLE II.2

Parameters of PE 05

Frequency	**0 Hz**	**10 kHz**	**20 kHz**	**40 kHz**	**100 kHz**	**150 kHz**	**200 kHz**	**400 kHz**	**500 kHz**
R' (Ω/km)	172	172	173	175	190	207	227	302	334
L' (µH/km)	680	678	675	667	646	637	629	603	592
C' (nF/km)	25	25	25	25	25	25	25	25	25

TABLE II.3

Parameters of PE 06

Frequency	**0 Hz**	**10 kHz**	**20 kHz**	**40 kHz**	**100 kHz**	**150 kHz**	**200 kHz**	**400 kHz**	**500 kHz**
R' (Ω/km)	119	120	121	125	146	167	189	260	288
L' (µH/km)	700	695	693	680	655	641	633	601	590
C' (nF/km)	56	56	56	56	56	56	56	56	56

TABLE II.4

Parameters of PE 08

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω/km)	67	70	72.5	75.0	91.7	105	117	159	177.5
L' (µH/km)	700	700	687	665	628	609	595	568	543
C' (nF/km)	37.8	37.8	37.8	37.8	37.8	37.8	37.8	37.8	37.8

TABLE II.5

Parameters of PVC 032

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω/km)	419	419	419	419	427	453	493	679	750
L' (µH/km)	650	650	650	650	647	635	621	577	560
C' (nF/km)	120	120	120	120	120	120	120	120	120

TABLE II.6

Parameters of PVC 04

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω/km)	268	268	268	268	281	295	311	391	426
L' (µH/km)	650	650	650	650	635	627	619	592	579
C' (nF/km)	120	120	120	120	120	120	120	120	120

TABLE II.7

Parameters of PVC 063

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω/km)	108	108	108	111	141	173	207	319	361
L' (µH/km)	635	635	635	630	604	584	560	492	469
C' (nF/km)	120	120	120	120	120	120	120	120	120

APPENDIX III

Signal Regenerator Startup Description (Informative)

This appendix describes the startup sequence used on spans employing regenerators. The sequence applies to spans with an arbitrary number of regenerators (up to 8), but for simplicity, the description here assumes a two-regenerator link. The use of line probing is optional, but its use is assumed for the purpose of this description.

The basic premise is that capability lists and line probe results propagate from the STU-R toward the STU-C and that the SHDSL training begins at the STU-C and propagates in the direction toward the STU-R. The Regenerator Silent Period (RSP) bit in G.994.1 is used to hold off segments while the startup process propagates across the span.

The block diagram in Figure III-1 shows a typical SHDSL span with two regenerators as a reference for the startup sequences described below.

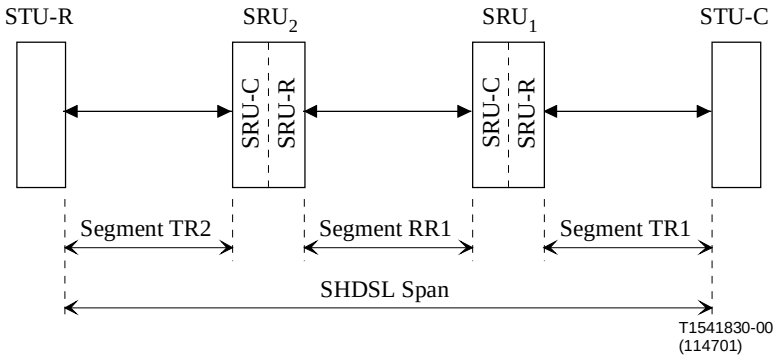

FIGURE III-1

Block Diagram of a SHDSL Span with Two Signal Regenerators

III.1 STU-R Initiated Startup

In most typical SHDSL installations, the STU-R can be expected to initiate the startup process. The proposed SHDSL startup process for STU-R initiation is described in the text below and shown graphically in Table III-1.

In this mode, the STU-R triggers the startup process by initiating a G.994.1 session with the regenerator closest to it (over segment TR2). The STU-R and the SRU_2-C then exchange capabilities and optionally perform a line probe and a second capabilities exchange. The units do not have enough information to begin SHDSL activation at this point, so the SRU_2-C issues an MS with the RSP bit set to hold off the STU-R while the startup process propagates across the span. The G.994.1 session terminates normally, and the STU-R begins its waiting period.

Next, the SRU_2-C conveys the capabilities from Segment TR2 to the SRU_2-R across the regenerator's internal interface. The SRU_2-R then initiates a G.994.1 session with the SRU_1-C and performs the same capabilities exchange and line probing sequence described above for the first segment. The capabilities expressed by the SRU_2-R are the intersection of its own capabilities with the capabilities it has received for Segment TR2. The units still do not have sufficient information

to begin SHDSL activation, so, again, the SRU_1-R issues an MS with the RSP bit set. The G.994.1 session terminates normally, and the SRU_2-R begins its waiting period.

As before, the SRU_1-C then conveys the capabilities from Segment RR1 (including the information from Segment TR2) to the SRU_1-R across the regenerator's internal interface. The SRU_1-R initiates a G.994.1 session with the STU-C and performs a capabilities exchange. Optionally, a line probe and a second capabilities exchange may be used. As before, the capabilities expressed by the SRU_1-R are the intersection of its own capabilities with the capabilities it has received for Segments RR1 and TR2. At this point, the STU-C possesses all of the required information to select the span's operational parameters. The data rate and other parameters are selected, just as in a normal (non-regenerator) preactivation sequence and then the SHDSL activation begins for Segment TR1.

When the STU-C / SRU_1-R link (over Segment TR1) has completed the SHDSL activation sequence (or the G.994.1 session, if clock mode 1 is selected), the SRU_1-R communicates the selected operational parameters to the SRU_1-C across the regenerator's internal interface. At this point, the SRU_1-C initiates a G.994.1 session with the SRU_2-R over Segment RR1. Parameters are selected -- there should be no need for another CLR-CL exchange at this point -- and the units perform the normal SHDSL activation. If clock mode 1 is selected (classic plesiochronous) there is no need to lock symbol timing to a network clock reference. In this case, the SRU_1-C / SRU_2-R G.994.1 session and activation should begin as soon as the STU-C / SRU_1-R G.994.1 sessions completes. In clock modes 2, 3a, and 3b, such a network or data clock reference is necessary for establishing symbol timing. In these modes, the SRU_1-C will delay the initiation of its G.994.1 session until the STU-C / SRU_1-R activation is complete. In this way, the required reference clock will be available for symbol timing on the SRU_1-C / SRU_2-R segment.

When the SRU_1-C / SRU_2-R link (over Segment RR1) has completed the SHDSL activation sequence (or the G.994.1 session, if clock mode 1 is selected), the SRU_2-R communicates the selected operational parameters to the SRU_2-C across the regenerator's internal interface. The SRU_2-C initiates a G.994.1 session with the STU-R over Segment TR2. Parameters are selected and the units perform the normal SHDSL activation. When this activation sequence is complete, the span can become fully operational.

TABLE III-1

STU-R Initiated Startup Sequence

Segment TR2 (STU-R / SRU_2-C)	Segment RR1 (SRU_2-R / SRU_1-C)	Segment TR1 (SRU_1-R / STU-C)
G.994.1 Start →		
Capabilities exchange		
Line probe		
Capabilities exchange		
← MS (RSP)		
	G.994.1 Start →	
	Capabilities exchange	
	Line probe	
	Capabilities exchange	
	← MS (RSP)	
		G.994.1 Start →
		Capabilities exchange
		Line probe
		Capabilities exchange
		Mode Selection
		SHDSL activation
	← G.994.1 Start	
	Mode Selection	
	SHDSL activation	
← G.994.1 Start		
Mode Selection		
SHDSL activation		

III.2 STU-C Initiated Startup

In some cases, it may be desirable for the STU-C to initiate the startup process. The proposed SHDSL startup process for STU-C initiation is described in the text below and shown graphically in Table III-2.

In this mode, the STU-C triggers the startup process by initiating a G.994.1 session with the regenerator closest to it (over segment TR1). The SRU_2-C issues an MS with the RSP bit set to hold off the STU-C while the startup process propagates across the span. The G.994.1 session terminates normally, and the STU-C begins its wait period. Next, the SRU_1-C initiates a G.994.1 session with the SRU_2-R, which, again is terminated following an MS from the SRU_2-R with the RSP bit set.

The SRU_2-C next initiates a G.994.1 session with the STU-R. From this point on, the start sequence is as described in § III.1 for the STU-R initiated startup.

TABLE III-2

STU-C Initiated Startup Sequence

Segment TR2 (STU-R / SRU_2-C)	Segment RR1 (SRU_2-R / SRU_1-C)	Segment TR1 (SRU_1-R / STU-C)
		← G.994.1 Start
		MS (RSP) →
	← G.994.1 Start	
	MS (RSP) →	
← G.994.1 Start		
Capabilities exchange		
Line probe		
Capabilities exchange		
← MS (RSP)		
	G.994.1 Start →	
	Capabilities exchange	
	Line probe	
	Capabilities exchange	
	← MS (RSP)	
		G.994.1 Start →
		Capabilities exchange
		Line probe
		Capabilities exchange
		Mode Selection
		SHDSL activation
	← G.994.1 Start	
	Mode Selection	
	SHDSL activation	
← G.994.1 Start		
Mode Selection		
SHDSL activation		

III.3 SRU Initiated Startup

In some limited applications (including some maintenance and retrain scenarios), it may be desirable for a regenerator to initiate the start sequence. In this mode, the SRU will initiate the train in the downstream direction – i.e., toward the STU-R in the same manner that it would have for the corresponding segment of the STU-C Startup Procedure (as described in § III.2). The STU-R will then initiate the capabilities exchange and line probing procedure toward the STU-C, as in a normal

STU-C initiated startup. The startup sequence begins with the initiating SRU-C and propagating toward the STU-R.

III.4 Collisions and Retrains

Collisions (equivalent to "glare" conditions in voice applications) can occur in cases where both the STU-C and the STU-R attempt to initiate connections simultaneously. Using the process described above, these collisions are resolved by specifying that R-to-C capabilities exchanges and probes will always take precedence over C-to-R train requests. G.994.1 sessions inherently resolve collisions on individual segments.

In G.994.1, the RSP timeout is specified as approximately 1 minute. For spans with no more than one regenerator, this is ideal. For multi-regenerator spans, however, an STU may time out and initiate a new G.994.1 session before the SRU is prepared to begin the next phase of the train. In such cases, the SRU should respond to the G.994.1 initiation and issue an MS message with the RSP bit set to hold off the STU once again. For its part, the SRU should implement an internal timer and should not consider a startup to have failed until that timer has expired. The timer should be started when the SRU receives a RSP bit in an MS message and should not expire for at least 4 minutes.

If any segment must retrain due to line conditions or other causes, each segment of the span shall be deactivated and the full startup procedure shall be reinitiated.

III.5 Diagnostic Mode Activation

If a segment fails, the startup procedure will also fail for the entire span. This would normally be characterized at the STU by being told to enter a silent interval via the RSP bit and never receiving another G.994.1 request. Without some diagnostic information, the service provider would have no easy way to test the integrity of the various segments.

This concern is resolved by the use of the "Diagnostic Mode" in G.994.1 to trigger a diagnostic training mode. This bit, when set, causes an SRU connected to a failed segment to act as an STU and allow the startup procedure to finish. In this way, all of the segments before the failed segment may be tested using loopbacks and EOC-initiated tests, allowing network operators to quickly isolate the segment where the failure has occurred.

APPENDIX IV

Bibliography

[B1] ITU-T Recommendation G.961 - Digital transmission system on metallic local lines for ISDN basic rate access.

[B2] ITU-T Recommendation G.995.1 - Recommendation G.995.1 (06/99) - Overview of digital subscriber line (DSL) Recommendations.

[B3] ANSI X3.4-1986 (R1997) - Information Systems - Coded Character Sets - 7-Bit American National Standard Code for Information Interchange (7-Bit ASCII).

[B4] ITU-T Recommendation K.50 - Safe Limits of Operating Voltages and Currents for Telecommunication Systems Powered over the Network.

[B5] Telcordia Technologies, GR-1089-CORE - Electromagnetic Compatibility and Electrical Safety (February 1999).

[B6] ITU-T Recommendation G.704 - Synchronous frame structures used at 1 544, 6 312, 2 048, 8 448 and 44 736 kbit/s hierarchical levels.

[B7] ANSI/IEEE Std 455-1985 - IEEE Standard Test Procedure for Measuring Longitudinal Balance of Telephone Equipment Operating in the Voice Band.

[B8] ITU-T Recommendation O.9 - Measuring Arrangements to Assess the Degree of Unbalance About Earth.

[B9] IETF RFC 2495 - Definitions of Managed Objects for the DS1, E1, DS2 and E2 Interface Types.